



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint®2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019

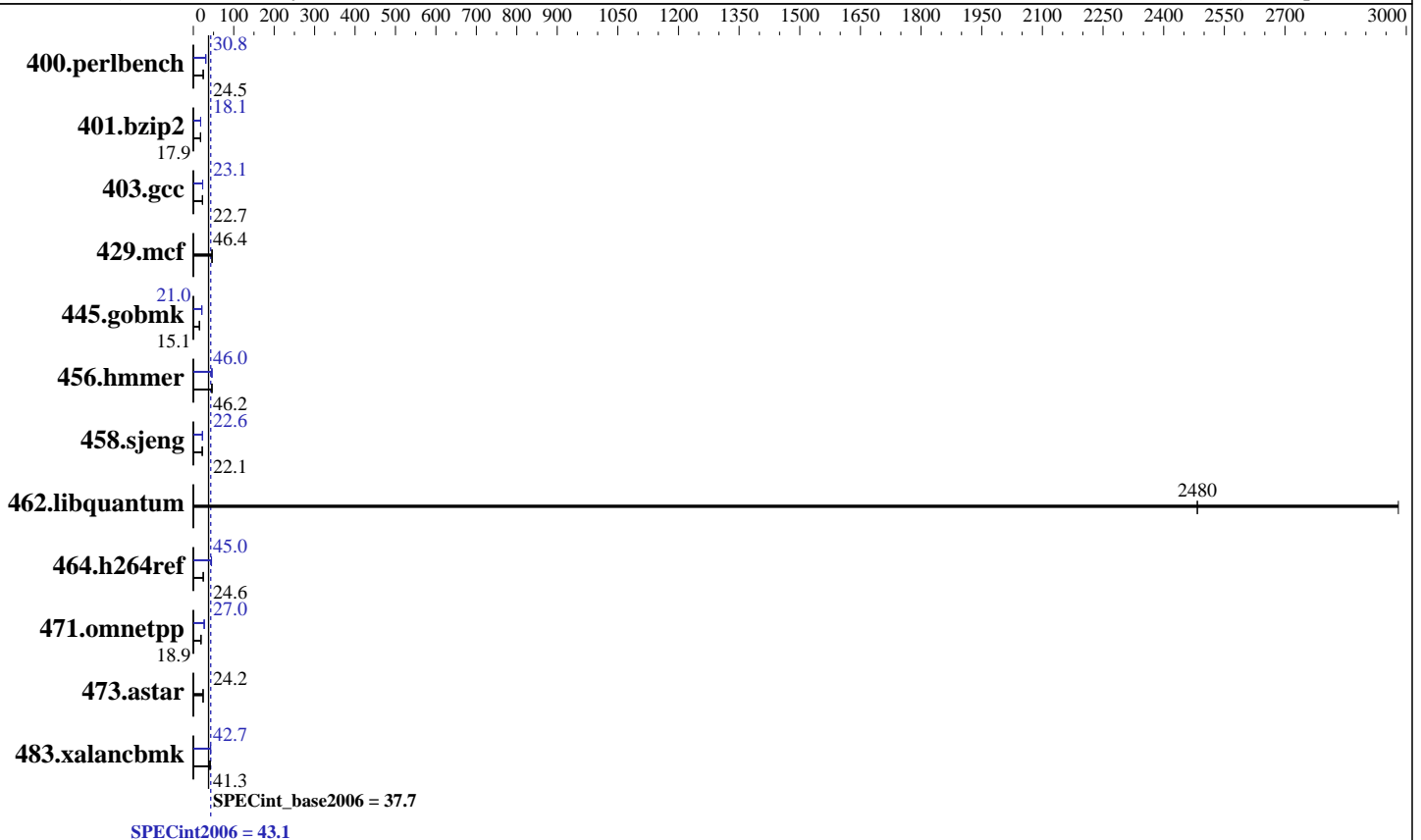
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Jul-2014

Hardware Availability: May-2014

Software Availability: Apr-2014



Hardware

CPU Name: Intel Xeon E7-4830 v2
CPU Characteristics: Intel Turbo Boost Technology up to 2.70 GHz
CPU MHz: 2200
FPU: Integrated
CPU(s) enabled: 40 cores, 4 chips, 10 cores/chip, 2 threads/core
CPU(s) orderable: 1,2,3,4 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 20 MB I+D on chip per chip
Other Cache: None
Memory: 512 GB (64 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1066 MHz and CL11)
Disk Subsystem: 1 X 300 GB 15000 RPM SAS
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
 2.6.32-431.el6.x86_64
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: Yes
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jul-2014
Hardware Availability: May-2014
Software Availability: Apr-2014

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	399	24.5	398	24.6	398	24.5	317	30.8	318	30.8	318	30.7
401.bzip2	540	17.9	540	17.9	541	17.9	533	18.1	533	18.1	533	18.1
403.gcc	355	22.7	355	22.7	355	22.7	348	23.1	348	23.1	348	23.1
429.mcf	196	46.6	197	46.4	198	46.0	196	46.6	197	46.4	198	46.0
445.gobmk	693	15.1	694	15.1	692	15.2	500	21.0	500	21.0	500	21.0
456.hammer	201	46.3	202	46.2	205	45.6	203	46.0	203	46.0	203	46.0
458.sjeng	547	22.1	547	22.1	547	22.1	535	22.6	535	22.6	535	22.6
462.libquantum	8.34	2480	8.35	2480	6.95	2980	8.34	2480	8.35	2480	6.95	2980
464.h264ref	900	24.6	899	24.6	899	24.6	492	45.0	492	45.0	492	44.9
471.omnetpp	329	19.0	330	18.9	331	18.9	230	27.2	232	27.0	233	26.8
473.astar	290	24.2	290	24.2	292	24.0	290	24.2	290	24.2	292	24.0
483.xalancbmk	164	42.1	170	40.5	167	41.3	162	42.6	162	42.7	161	42.8

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

```

Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disabled
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
Sysinfo program /opt/cpu2006-1.4/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on B460M4 Thu Jul 17 19:31:19 2014
This section contains SUT (System Under Test) info as seen by
some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo
From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7-4830 v2 @ 2.20GHz
4 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12

```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jul-2014
Hardware Availability: May-2014
Software Availability: Apr-2014

Platform Notes (Continued)

```

physical 1: cores 0 1 2 3 4 8 9 10 11 12
physical 2: cores 0 1 2 3 4 8 9 10 11 12
physical 3: cores 0 1 2 3 4 8 9 10 11 12
cache size : 20480 KB
From /proc/meminfo
MemTotal:      528550804 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)
From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server
uname -a:
Linux B460M4 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013 x86_64
x86_64 x86_64 GNU/Linux
run-level 3 Jul 15 20:59
SPEC is set to: /opt/cpu2006-1.4
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        ext4  275G  85G  176G  33% /
Additional information from dmidecode:
BIOS Cisco Systems, Inc. EXM4-1.2.2.1.21.042220141009 04/22/2014
Memory:
64x 8 GB
64x 0xCE00 M393B1K70QB0-YK0 8 GB 1066 MHz 2 rank
32x NO DIMM NO DIMM
(End of data from sysinfo program)

```

General Notes

Environment variables set by runspec before the start of the run:

```

KMP_AFFINITY = "granularity=fine,compact,1,0"
LD_LIBRARY_PATH = "/opt/cpu2006-1.4/libs/32:/opt/cpu2006-1.4/libs/64:/opt/cpu2006-1.4/sh"
OMP_NUM_THREADS = "80"

```

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4

Transparent Huge Pages enabled with:

```

echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled

```

runspec command invoked through numactl i.e.:

```

numactl --interleave=all runspec <etc>

```

Submitted_by: "Sheshgiri I (shei)" <shei@cisco.com>

Submitted: Wed Jul 23 14:31:05 EDT 2014

Submission: cpu2006-20140723-30549.sub

Base Compiler Invocation

C benchmarks:
icc -m64

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jul-2014
Hardware Availability: May-2014
Software Availability: Apr-2014

Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32
C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64
400.perlbench: icc -m32
445.gobmk: icc -m32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Jul-2014

Hardware Availability: May-2014

Software Availability: Apr-2014

Peak Compiler Invocation (Continued)

464.h264ref: icc -m32

C++ benchmarks (except as noted below):

icpc -m32

473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
 401.bzip2: -DSPEC_CPU_LP64
 403.gcc: -DSPEC_CPU_LP64
 429.mcf: -DSPEC_CPU_LP64
 456.hmmer: -DSPEC_CPU_LP64
 458.sjeng: -DSPEC_CPU_LP64
 462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
 473.astar: -DSPEC_CPU_LP64
 483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -opt-prefetch -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
 -opt-prefetch -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div -inline-calloc
 -opt-malloc-options=3 -auto-ilp32

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
 -ansi-alias

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
 -ansi-alias

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -unroll4

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

SPECint2006 = 43.1

SPECint_base2006 = 37.7

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Jul-2014

Hardware Availability: May-2014

Software Availability: Apr-2014

Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-ra-region-strategy=block -ansi-alias
-Wl,-z,muldefs -L/sh -lsmarheap

473.astar: basepeak = yes

483.xalancbmk: -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -ansi-alias
-Wl,-z,muldefs -L/sh -lsmarheap

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Tue Aug 12 13:15:45 2014 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 12 August 2014.