



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint®_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

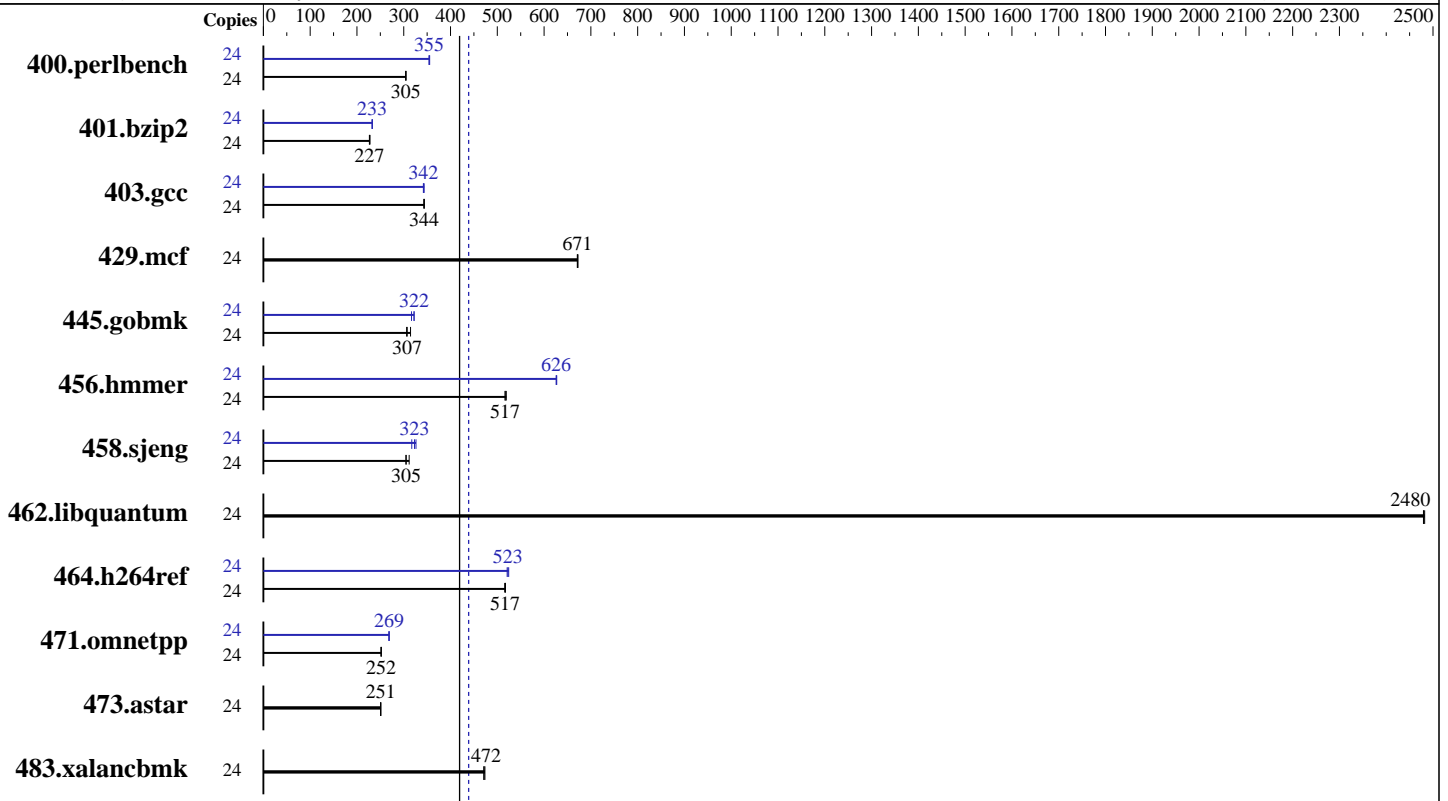
Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011



SPECint_rate2006 = 439

SPECint_rate_base2006 = 419

Hardware

CPU Name: Intel Xeon E5-2630
 CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz
 CPU MHz: 2300
 FPU: Integrated
 CPU(s) enabled: 12 cores, 2 chips, 6 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2 chip
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 15 MB I+D on chip per chip
 Other Cache: None
 Memory: 128 GB (16 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1333 MHz and CL7)
 Disk Subsystem: 1 X 300 GB 10000 RPM SAS
 Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)
 2.6.32-220.el6.x86_64
 Compiler: C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
 Auto Parallel: No
 File System: ext4
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V9.01



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	24	770	305	771	304	769	305	24	660	355	662	354	661	355
401.bzip2	24	1020	227	1017	228	1022	227	24	995	233	995	233	996	232
403.gcc	24	562	344	562	344	563	343	24	564	342	562	344	565	342
429.mcf	24	326	671	326	671	325	673	24	326	671	326	671	325	673
445.gobmk	24	822	306	800	315	819	307	24	795	317	782	322	781	322
456.hammer	24	433	517	433	517	431	519	24	358	626	357	627	358	626
458.sjeng	24	954	305	932	312	951	305	24	899	323	916	317	890	326
462.libquantum	24	200	2480	201	2480	201	2480	24	200	2480	201	2480	201	2480
464.h264ref	24	1030	516	1027	517	1026	517	24	1016	523	1013	524	1019	521
471.omnetpp	24	596	252	596	252	596	252	24	558	269	558	269	559	268
473.astar	24	673	250	671	251	671	251	24	673	250	671	251	671	251
483.xalancbmk	24	351	471	351	472	350	474	24	351	471	351	472	350	474

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuration:

Intel(R) Hyper-Threading Technology set to Enabled

Processor Power State C6 set to Disabled

Processor Power State C1 Enhanced set to Disabled

Power Technology set to Custom

Energy Performance set to Performance

DRAM Clock Throttling set to Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800

\$Rev: 6800 \$ \$Date:: 2011-10-11 #\$ 6f2ebdff5032aaa42e583f96b07f99d3

running on localhost.localdomain Tue Apr 3 02:44:02 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E5-2630 0 @ 2.30GHz

Continued on next page

Standard Performance Evaluation Corporation

info@spec.org

<http://www.spec.org/>



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Platform Notes (Continued)

```

2 "physical id"s (chips)
24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 6
siblings  : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
cache size : 15360 KB

From /proc/meminfo
MemTotal:      132101560 kB
HugePages_Total: 0
Hugepagesize:  2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

uname -a:
Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13
EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 3 02:37

SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sdal       ext4      275G  9.9G  251G   4% /

Additional information from dmidecode:
Memory:
16x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 1 rank

(End of data from sysinfo program)

```

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Base Compiler Invocation

C benchmarks:

icc -m32

C++ benchmarks:

icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
 401.bzip2: -DSPEC_CPU_LP64
 456.hmmer: -DSPEC_CPU_LP64
 458.sjeng: -DSPEC_CPU_LP64
 462.libquantum: -DSPEC_CPU_LINUX
 483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
 -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
 -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
 -L/smartheap -lsmartheap

473.astar: basepeak = yes

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

SPECint_rate2006 = 439

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

SPECint_rate_base2006 = 419

CPU2006 license: 9019

Test date: Apr-2012

Test sponsor: Cisco Systems

Hardware Availability: Jun-2012

Tested by: Cisco Systems

Software Availability: Dec-2011

Peak Optimization Flags (Continued)

483.xalanbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Thu Jul 24 04:44:20 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 9 May 2012.