SPEC® CINT2006 Result
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Cisco Systems

Cisco UCS C460 M4 (Intel Xeon E7-4850 v3, 2.20 GHz)

$SPECint^{®}\_rate2006 =$ Not Run

$SPECint\_rate\_base2006 =$ 1970

SPECint_rate_base2006 = 1970

Benchmark	Copies	Score
400.perlbench	112	1520
401.bzip2	112	957
403.gcc	112	1490
429.mcf	112	2470
445.gobmk	112	1430
456.hmmer	112	2910
458.sjeng	112	1500
462.libquantum	112	19600
464.h264ref	112	2440
471.omnetpp	112	916
473.astar	112	1080
483.xalancbmk	112	2110

Hardware

CPU Name: Intel Xeon E7-4850 v3
CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz
CPU MHz: 2200
FPU: Integrated
CPU(s) enabled: 56 cores, 4 chips, 14 cores/chip, 2 threads/core
CPU(s) orderable: 2,4 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 35 MB I+D on chip per chip
Other Cache: None
Memory: 1 TB (64 x 16 GB 2Rx4 PC4-2133P-R, running at 1333 MHz)
Disk Subsystem: 1 x 600 GB SAS, 10K RPM
Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 12 (x86_64) 3.12.28-4-default
Compiler: C/C++: Version 15.0.0.090 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0

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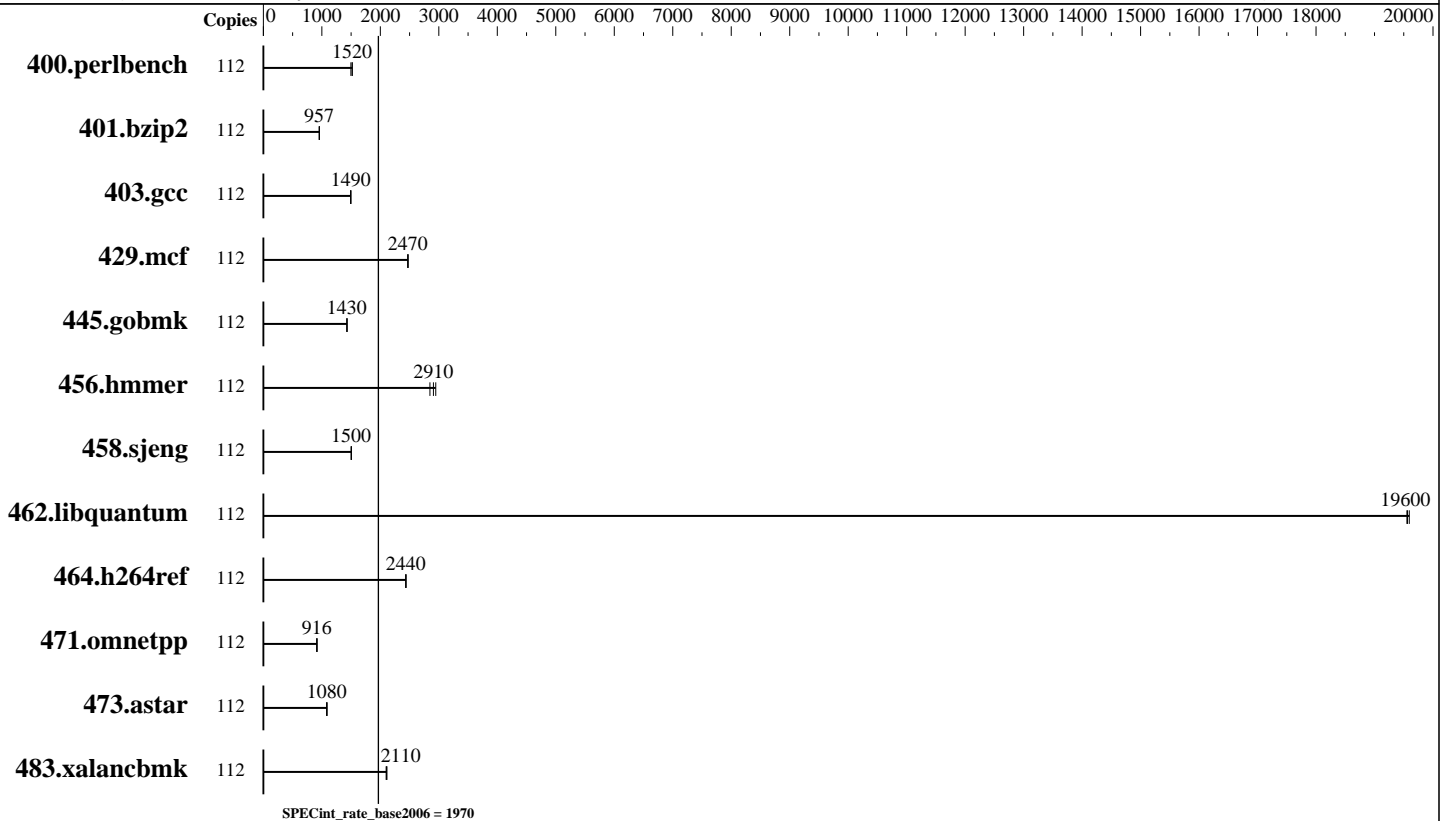
CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jul-2015
Hardware Availability: May-2015
Software Availability: Nov-2014

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	112	720	1520	731	1500	**720**	**1520**							
401.bzip2	112	1129	957	**1130**	**957**	1130	956							
403.gcc	112	604	1490	**604**	**1490**	602	1500							
429.mcf	112	**413**	**2470**	414	2470	413	2470							
445.gobmk	112	822	1430	823	1430	**822**	**1430**							
456.hmmer	112	355	2950	367	2850	**359**	**2910**							
458.sjeng	112	**901**	**1500**	902	1500	901	1500							
462.libquantum	112	119	19600	**119**	**19600**	118	19600							
464.h264ref	112	1018	2430	1016	2440	**1017**	**2440**							
471.omnetpp	112	**764**	**916**	768	911	763	917							
473.astar	112	722	1090	726	1080	**726**	**1080**							
483.xalancbmk	112	368	2100	366	2110	**367**	**2110**							

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

    The numactl mechanism was used to bind copies to processors. The config file option 'submit'
    was used to generate numactl commands to bind each copy to a specific processor.
    For details, please see the config file.

Operating System Notes

    Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    BIOS Configuration:
    CPU performance set to Enterprise
    Power Technology set to Performance
    Energy Performance BIAS setting set to Balanced Performance
    Memory RAS configuration set to Maximum Performance
    Memory Power Saving Mode set to Disabled
     Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
     $Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
     running on sles12 Mon Jul 6 02:34:59 2015

     This section contains SUT (System Under Test) info as seen by
     some common utilities. To remove or add to this section, see:
       http://www.spec.org/cpu2006/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) CPU E7-4850 v3 @ 2.20GHz
           4 "physical id"s (chips)

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Platform Notes (Continued)

```
     112 "processors"
  cores, siblings (Caution: counting these is hw and system dependent.  The
  following excerpts from /proc/cpuinfo might not be reliable.  Use with
  caution.)
     cpu cores : 14
     siblings  : 28
     physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
     physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
     physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
     physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
  cache size : 35840 KB

From /proc/meminfo
  MemTotal:       1058662276 kB
  HugePages_Total:        0
  Hugepagesize:        2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
     SUSE Linux Enterprise Server 12 (x86_64)
     VERSION = 12
     PATCHLEVEL = 0
     # This file is deprecated and will be removed in a future service pack or
     release.
     # Please check /etc/os-release for details about this release.
  os-release:
     NAME="SLES"
     VERSION="12"
     VERSION_ID="12"
     PRETTY_NAME="SUSE Linux Enterprise Server 12"
     ID="sles"
     ANSI_COLOR="0;32"
     CPE_NAME="cpe:/o:suse:sles:12"

uname -a:
  Linux sles12 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014 (9879bd4)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jul 6 02:23

SPEC is set to: /opt/cpu2006-1.2
  Filesystem      Type  Size  Used Avail Use% Mounted on
  /dev/sda2       xfs   500G  104G  397G  21% /
Additional information from dmidecode:

  Warning: Use caution when you interpret this section. The 'dmidecode' program
  reads system data which is "intended to allow hardware to be accurately
  determined", but the intent may not be met, as there are frequent changes to
  hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. C460M4.2.0.5b.0.052420152246 05/24/2015
  Memory:
```

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Platform Notes (Continued)

```
     64x 0xCE00 M393A2G40DB0-CPB 16 GB 2 rank 1333 MHz
     32x NO DIMM NO DIMM   1333 MHz

  (End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

 Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB
 memory using RedHat EL 7.0
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/transparent_hugepage/enabled
 Filesystem page cache cleared with:
 echo 1>       /proc/sys/vm/drop_caches
 runspec command invoked through numactl i.e.:
 numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
```
    icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
```

C++ benchmarks:
```
    icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
```

Base Portability Flags

```
    400.perlbench: -DSPEC_CPU_LINUX_IA32
    462.libquantum: -DSPEC_CPU_LINUX
    483.xalancbmk: -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:
```
    -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
    -opt-mem-layout-trans=3
```

C++ benchmarks:
```
    -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
    -opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap
```

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Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150729.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150729.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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