SPEC® CINT2006 Result

Cisco Systems

Cisco UCS C240 M4 (Intel Xeon E5-2620 v4 2.10 GHz)

$SPECint^{®}\_rate2006 = 663$

$SPECint\_rate\_base2006 = 630$

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2016
Hardware Availability: Apr-2016
Software Availability: Dec-2015

| Copies | 0 | 200 | 400 | 600 | 800 | 1100 | 1400 | 1700 | 2000 | 2300 | 2600 | 2900 | 3200 | 3500 | 3800 | 4100 | 4400 | 4700 | 5000 | 5300 | 5600 | 6200 |

400.perlbench 32 542 32 435
401.bzip2 32 308 32 297
403.gcc 32 482 32 480
429.mcf 32 884
445.gobmk 32 404 32 395
456.hmmer 32 1110 32 910
458.sjeng 32 434 32 410
462.libquantum 32 6110
464.h264ref 32 753 32 740
471.omnetpp 32 370 32 347
473.astar 32 380
483.xalancbmk 32 809

SPECint_rate_base2006 = 630

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Hardware

CPU Name:	Intel Xeon E5-2620 v4
CPU Characteristics:	Intel Turbo Boost Technology up to 3.00 GHz
CPU MHz:	2100
FPU:	Integrated
CPU(s) enabled:	16 cores, 2 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable:	2,4 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	20 MB I+D on chip per chip
Other Cache:	None
Memory:	256 GB (16 x 16 GB 2Rx4 PC4-2400T-R, running at 2133 MHz)
Disk Subsystem:	1 x 400 GB SAS SSD
Other Hardware:	None

Software

Operating System:	SUSE Linux Enterprise Server 12 SP1 (x86_64) 3.12.49-11-default
Compiler:	C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux
Auto Parallel:	No
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.2

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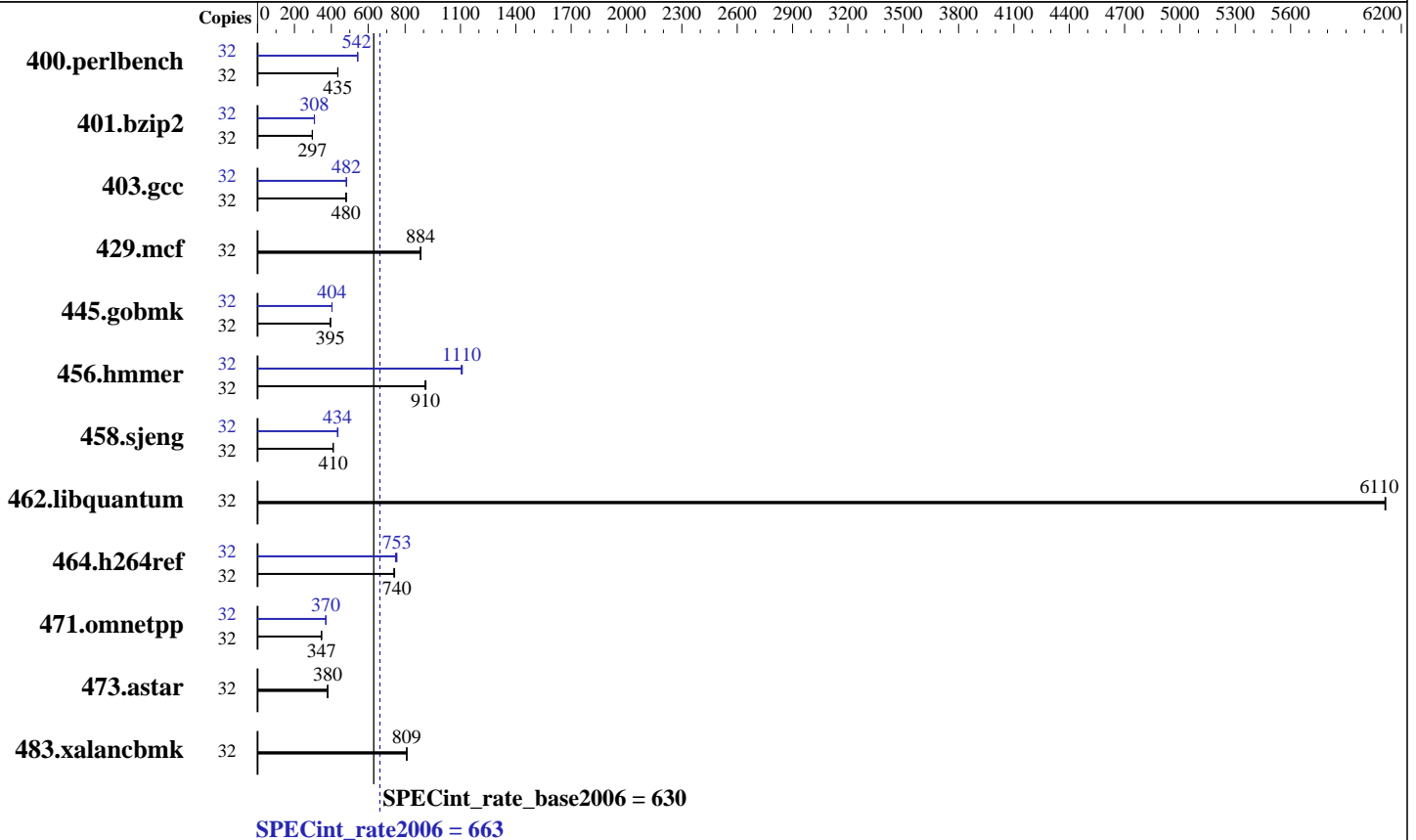
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Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	32	718	436	**718**	**435**	720	434	32	**576**	**542**	575	543	577	542
401.bzip2	32	1041	297	1038	297	**1040**	**297**	32	1004	308	1001	309	**1002**	**308**
403.gcc	32	**537**	**480**	538	479	535	482	32	536	481	**535**	**482**	533	483
429.mcf	32	**330**	**884**	331	882	330	885	32	**330**	**884**	331	882	330	885
445.gobmk	32	**849**	**395**	850	395	849	396	32	832	404	**832**	**404**	832	403
456.hmmer	32	327	913	329	908	**328**	**910**	32	270	1100	**270**	**1110**	269	1110
458.sjeng	32	943	410	**945**	**410**	946	409	32	889	436	**892**	**434**	894	433
462.libquantum	32	108	6110	108	6110	**108**	**6110**	32	108	6110	108	6110	**108**	**6110**
464.h264ref	32	953	743	958	739	**956**	**740**	32	**940**	**753**	947	748	937	755
471.omnetpp	32	577	346	**577**	**347**	577	347	32	**540**	**370**	540	370	540	371
473.astar	32	592	380	**591**	**380**	591	380	32	592	380	**591**	**380**	591	380
483.xalancbmk	32	**273**	**809**	273	810	273	808	32	**273**	**809**	273	810	273	808

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

   The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

   Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    BIOS Settings:
    CPU performance set to Enterprise
    Power Technology set to Performance
    Energy Performance BIAS setting set to Balanced Performance
    Memory RAS configuration set to Maximum Performance
    Memory Power Saving Mode set to Disabled
    QPI Snoop Mode set to Home Directory Snoop with OSB
     Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
     $Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
     running on linux-0ezz Thu Nov 24 01:02:19 2016

     This section contains SUT (System Under Test) info as seen by
     some common utilities. To remove or add to this section, see:
       http://www.spec.org/cpu2006/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) CPU E5-2620 v4 @ 2.10GHz

Continued on next page

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Platform Notes (Continued)

```
    2 "physical id"s (chips)
    32 "processors"
 cores, siblings (Caution: counting these is hw and system dependent.  The
 following excerpts from /proc/cpuinfo might not be reliable.  Use with
 caution.)
    cpu cores : 8
    siblings  : 16
    physical 0: cores 0 1 2 3 4 5 6 7
    physical 1: cores 0 1 2 3 4 5 6 7
 cache size : 20480 KB

From /proc/meminfo
   MemTotal:       264568064 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 1
      # This file is deprecated and will be removed in a future service pack or
      release.
      # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP1"
      VERSION_ID="12.1"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp1"

uname -a:
   Linux linux-0ezz 3.12.49-11-default #1 SMP Wed Nov 11 20:52:43 UTC 2015
   (8d714a0) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Nov 24 00:22

SPEC is set to: /opt/cpu2006-1.2
   Filesystem      Type  Size  Used Avail Use% Mounted on
   /dev/sda1       xfs   372G   11G  362G   3% /
Additional information from dmidecode:

   Warning: Use caution when you interpret this section. The 'dmidecode' program
   reads system data which is "intended to allow hardware to be accurately
   determined", but the intent may not be met, as there are frequent changes to
   hardware, firmware, and the "DMTF SMBIOS" standard.

 BIOS Cisco Systems, Inc. C240M4.2.0.13d.0.0812161132 08/12/2016
 Memory:
   16x 0xCE00 M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz, configured at 2133 MHz
```

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Platform Notes (Continued)

```
    8x NO DIMM NO DIMM

 (End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

 Binaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB
 memory using RedHat EL 7.1
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/transparent_hugepage/enabled
 Filesystem page cache cleared with:
 echo 1>       /proc/sys/vm/drop_caches
 runspec command invoked through numactl i.e.:
 numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
```
    icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

C++ benchmarks:
```
    icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

Base Portability Flags

```
    400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
       401.bzip2: -D_FILE_OFFSET_BITS=64
         403.gcc: -D_FILE_OFFSET_BITS=64
         429.mcf: -D_FILE_OFFSET_BITS=64
       445.gobmk: -D_FILE_OFFSET_BITS=64
       456.hmmer: -D_FILE_OFFSET_BITS=64
       458.sjeng: -D_FILE_OFFSET_BITS=64
    462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
      464.h264ref: -D_FILE_OFFSET_BITS=64
     471.omnetpp: -D_FILE_OFFSET_BITS=64
        473.astar: -D_FILE_OFFSET_BITS=64
    483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:
```
    -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
    -opt-mem-layout-trans=3
```

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Base Optimization Flags (Continued)

C++ benchmarks:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap
```

Base Other Flags

C benchmarks:

  403.gcc: `-Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

  400.perlbench: `icc -m64`

   401.bzip2: `icc -m64`

   456.hmmer: `icc -m64`

   458.sjeng: `icc -m64`

C++ benchmarks:
```
icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
```

Peak Portability Flags

  400.perlbench: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
   401.bzip2: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64`
    403.gcc: `-D_FILE_OFFSET_BITS=64`
    429.mcf: `-D_FILE_OFFSET_BITS=64`
   445.gobmk: `-D_FILE_OFFSET_BITS=64`
   456.hmmer: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64`
   458.sjeng: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64`
  462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
   464.h264ref: `-D_FILE_OFFSET_BITS=64`
   471.omnetpp: `-D_FILE_OFFSET_BITS=64`
    473.astar: `-D_FILE_OFFSET_BITS=64`
  483.xalancbmk: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`

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Peak Optimization Flags

C benchmarks:

400.perlbench: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2)
`-par-num-threads=1`(pass 1) `-prof-use`(pass 2) `-auto-ilp32`

401.bzip2: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2)
`-par-num-threads=1`(pass 1) `-prof-use`(pass 2) `-opt-prefetch`
`-auto-ilp32 -ansi-alias`

403.gcc: `-xCORE-AVX2 -ipo -O3 -no-prec-div`

429.mcf: `basepeak = yes`

445.gobmk: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-prof-use`(pass 2) `-par-num-threads=1`(pass 1) `-ansi-alias`
`-opt-mem-layout-trans=3`

456.hmmer: `-xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32`

458.sjeng: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2)
`-par-num-threads=1`(pass 1) `-prof-use`(pass 2) `-unroll4`
`-auto-ilp32`

462.libquantum: `basepeak = yes`

464.h264ref: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2)
`-par-num-threads=1`(pass 1) `-prof-use`(pass 2) `-unroll2`
`-ansi-alias`

C++ benchmarks:

471.omnetpp: `-xCORE-AVX2`(pass 2) `-prof-gen:threadsafe`(pass 1)
`-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2)
`-par-num-threads=1`(pass 1) `-prof-use`(pass 2) `-ansi-alias`
`-opt-ra-region-strategy=block -Wl,-z,muldefs`
`-L/sh -lsmartheap`

473.astar: `basepeak = yes`

483.xalancbmk: `basepeak = yes`

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Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.xml

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