



# SPEC® CINT2006 Result

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## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6152, 2.10 GHz)

**SPECint®\_rate2006 = 4220**

**SPECint\_rate\_base2006 = 4040**

CPU2006 license: 9019

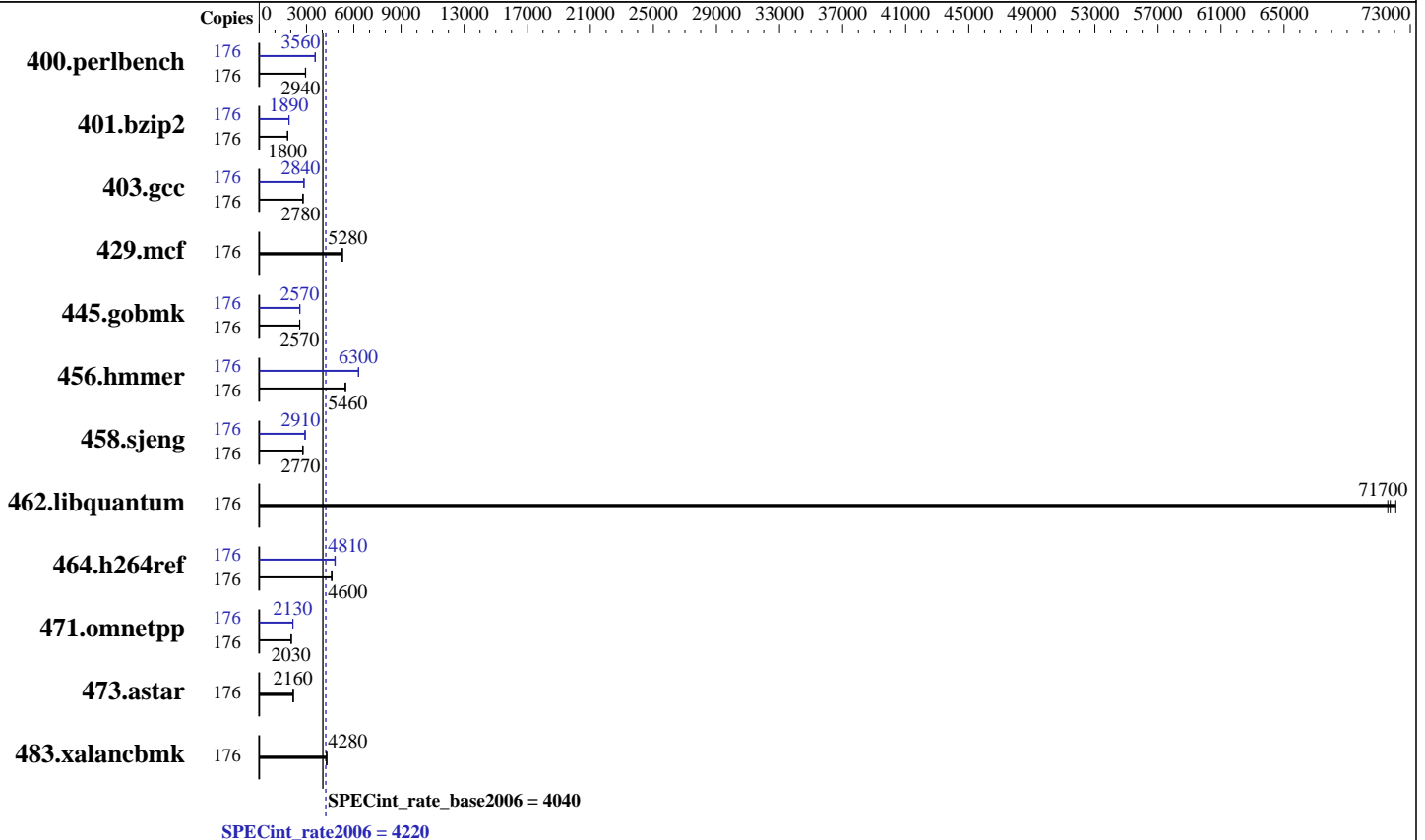
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Nov-2017

Hardware Availability: Aug-2017

Software Availability: Apr-2017



### Hardware

CPU Name: Intel Xeon Gold 6152  
 CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz  
 CPU MHz: 2100  
 FPU: Integrated  
 CPU(s) enabled: 88 cores, 4 chips, 22 cores/chip, 2 threads/core  
 CPU(s) orderable: 2,4 chips  
 Primary Cache: 32 KB I + 32 KB D on chip per core  
 Secondary Cache: 1 MB I+D on chip per core  
 L3 Cache: 30.25 MB I+D on chip per chip  
 Other Cache: None  
 Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)  
 Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM  
 Other Hardware: None

### Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.21-69-default  
 Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux  
 Auto Parallel: Yes  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 32-bit  
 Peak Pointers: 32/64-bit  
 Other Software: Microquill SmartHeap V10.2



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	176	584	2950	<b>584</b>	<b>2940</b>	587	2930	176	483	3560	<b>483</b>	<b>3560</b>	486	3540
401.bzip2	176	<b>941</b>	<b>1800</b>	947	1790	937	1810	176	899	1890	902	1880	<b>900</b>	<b>1890</b>
403.gcc	176	514	2760	509	2780	<b>509</b>	<b>2780</b>	176	<b>499</b>	<b>2840</b>	499	2840	501	2830
429.mcf	176	<b>304</b>	<b>5280</b>	305	5260	304	5280	176	<b>304</b>	<b>5280</b>	305	5260	304	5280
445.gobmk	176	718	2570	<b>718</b>	<b>2570</b>	720	2570	176	717	2580	718	2570	<b>717</b>	<b>2570</b>
456.hammer	176	301	5450	299	5480	<b>301</b>	<b>5460</b>	176	261	6290	260	6310	<b>261</b>	<b>6300</b>
458.sjeng	176	773	2760	765	2780	<b>770</b>	<b>2770</b>	176	<b>733</b>	<b>2910</b>	731	2910	733	2900
462.libquantum	176	<b>50.8</b>	<b>71700</b>	50.9	71600	50.6	72100	176	<b>50.8</b>	<b>71700</b>	50.9	71600	50.6	72100
464.h264ref	176	<b>847</b>	<b>4600</b>	847	4600	845	4610	176	812	4800	808	4820	<b>809</b>	<b>4810</b>
471.omnetpp	176	543	2030	542	2030	<b>542</b>	<b>2030</b>	176	<b>515</b>	<b>2130</b>	515	2140	515	2130
473.astar	176	575	2150	<b>573</b>	<b>2160</b>	572	2160	176	575	2150	<b>573</b>	<b>2160</b>	572	2160
483.xalancbmk	176	<b>284</b>	<b>4280</b>	284	4270	284	4280	176	<b>284</b>	<b>4280</b>	284	4270	284	4280

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Platform Notes

### BIOS Settings:

Intel HyperThreading Technology set to Enabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993  
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)  
running on linux-vb5q Sun Nov 26 00:00:09 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:  
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz  
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### Platform Notes (Continued)

```

4 "physical id"s (chips)
176 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 22
siblings  : 44
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27
28
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27
28
physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27
28
physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27
28
cache size : 30976 KB

```

```

From /proc/meminfo
MemTotal:      791027536 kB
HugePages_Total:      0
Hugepagesize:   2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

```

uname -a:
Linux linux-vb5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

```

run-level 3 Jan 4 10:20

```

SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal       xfs   280G   97G  184G  35% /

```

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately

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### Platform Notes (Continued)

determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017

Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

### General Notes

Environment variables set by runspec before the start of the run:

LD\_LIBRARY\_PATH = "/opt/intel/lib/ia32:/opt/intel/lib/intel64:/opt/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/transparent\_hugepage/enabled

Filesystem page cache cleared with:

shell invocation of 'sync; echo 3 > /proc/sys/vm/drop\_caches' prior to run runspec command invoked through numactl i.e.:

numactl --interleave=all runspec <etc>

### Base Compiler Invocation

C benchmarks:

icc -m32 -L/opt/intel/compilers\_and\_libraries\_2018/linux/lib/ia32

C++ benchmarks:

icpc -m32 -L/opt/intel/compilers\_and\_libraries\_2018/linux/lib/ia32

### Base Portability Flags

400.perlbench: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX\_IA32  
401.bzip2: -D\_FILE\_OFFSET\_BITS=64  
403.gcc: -D\_FILE\_OFFSET\_BITS=64  
429.mcf: -D\_FILE\_OFFSET\_BITS=64  
445.gobmk: -D\_FILE\_OFFSET\_BITS=64  
456.hmmer: -D\_FILE\_OFFSET\_BITS=64  
458.sjeng: -D\_FILE\_OFFSET\_BITS=64  
462.libquantum: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX  
464.h264ref: -D\_FILE\_OFFSET\_BITS=64  
471.omnetpp: -D\_FILE\_OFFSET\_BITS=64  
473.astar: -D\_FILE\_OFFSET\_BITS=64  
483.xalancbmk: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX



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## Base Optimization Flags

C benchmarks:  
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3

C++ benchmarks:  
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3  
-Wl,-z,muldefs -L/opt/cpu2006-1.2/sh10.2 -lsmartheap

## Base Other Flags

C benchmarks:  
403.gcc: -Dalloca=\_alloca

## Peak Compiler Invocation

C benchmarks (except as noted below):  
icc -m32 -L/opt/intel/compilers\_and\_libraries\_2018/linux/lib/ia32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:  
icpc -m32 -L/opt/intel/compilers\_and\_libraries\_2018/linux/lib/ia32

## Peak Portability Flags

400.perlbench: -DSPEC\_CPU\_LP64 -DSPEC\_CPU\_LINUX\_X64  
401.bzip2: -DSPEC\_CPU\_LP64  
403.gcc: -D\_FILE\_OFFSET\_BITS=64  
429.mcf: -D\_FILE\_OFFSET\_BITS=64  
445.gobmk: -D\_FILE\_OFFSET\_BITS=64  
456.hmmer: -DSPEC\_CPU\_LP64  
458.sjeng: -DSPEC\_CPU\_LP64  
462.libquantum: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX  
464.h264ref: -D\_FILE\_OFFSET\_BITS=64  
471.omnetpp: -D\_FILE\_OFFSET\_BITS=64  
473.astar: -D\_FILE\_OFFSET\_BITS=64  
483.xalancbmk: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX



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## Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32  
-qopt-mem-layout-trans=3

403.gcc: -xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: -xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32  
-qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2) -unroll4 -auto-ilp32  
-qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)  
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)  
-no-prec-div(pass 2)  
-qopt-ra-region-strategy=block  
-qopt-mem-layout-trans=3 -Wl,-z,muldefs  
-L/opt/cpu2006-1.2/sh10.2 -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes



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## Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=\_alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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