SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

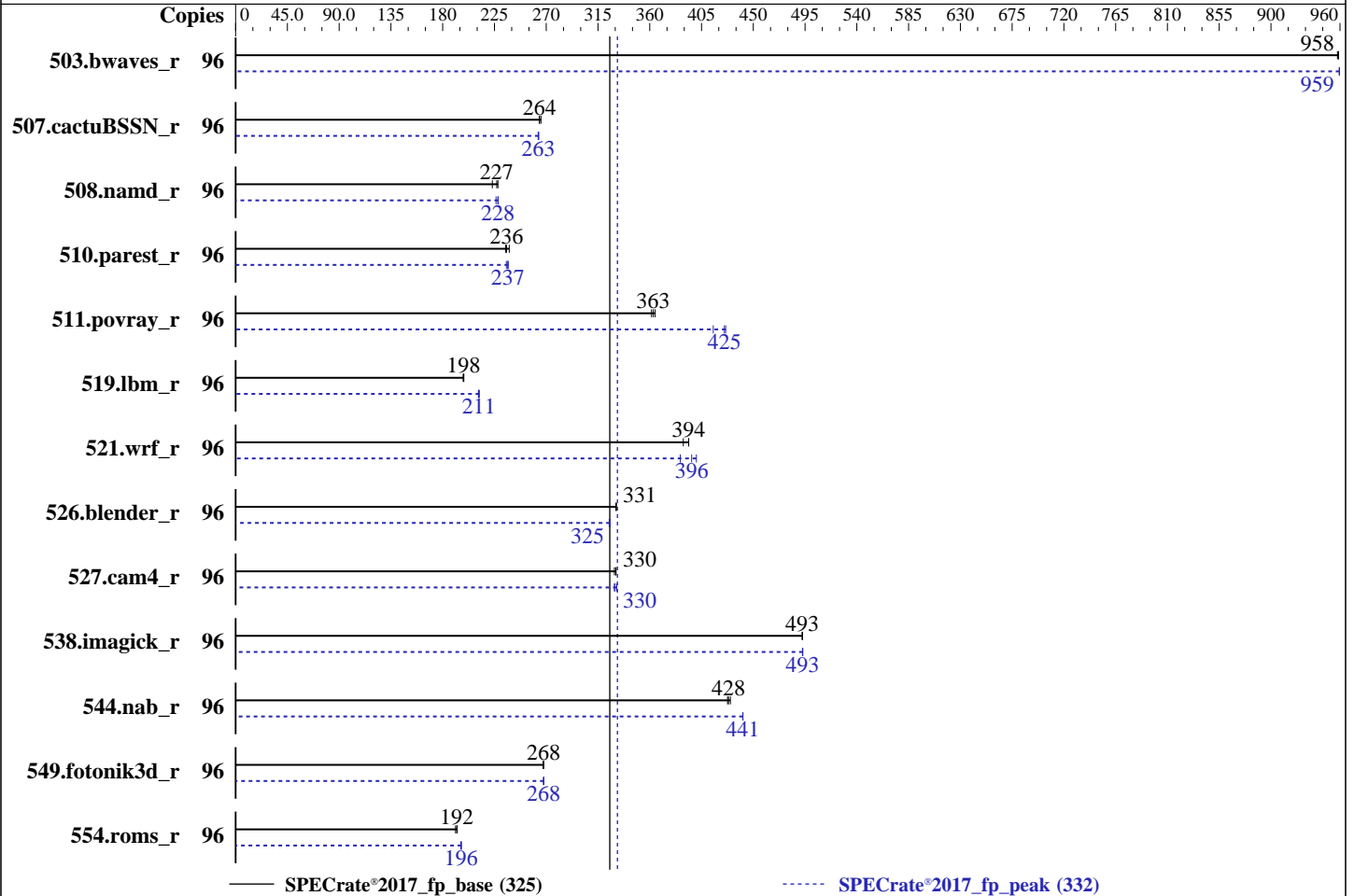SPECrate®2017_fp_peak = 332

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Benchmark	Copies	Base	Peak
503.bwaves_r	96	958	959
507.cactuBSSN_r	96	264	263
508.namd_r	96	227	228
510.parest_r	96	236	237
511.povray_r	96	363	425
519.lbm_r	96	198	211
521.wrf_r	96	394	396
526.blender_r	96	331	325
527.cam4_r	96	330	330
538.imagick_r	96	493	493
544.nab_r	96	428	441
549.fotonik3d_r	96	268	268
554.roms_r	96	192	196

—— SPECrate®2017_fp_base (325)   ----- SPECrate®2017_fp_peak (332)

Hardware

CPU Name: Intel Xeon Platinum 8158
 Max MHz: 3700
 Nominal: 3000
Enabled: 48 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 24.75 MB I+D on chip per chip
 Other: None
Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Storage: 2 x 1 TB SAS HDD, 7.2K RPM
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
4.4.21-69-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++
Compiler for Linux;
Fortran: Version 18.0.0.128 of Intel Fortran
Compiler for Linux
Parallel: No
Firmware: Version 3.1.0 released Jun-2017
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License:	9019	**Test Date:**	Oct-2017
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Sep-2017

Results Table

Benchmark	Base						Peak					
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	96	1004	959	1005	958	**1004**	**958**	96	**1003**	**959**	1003	959	1003	960
507.cactuBSSN_r	96	458	265	460	264	**460**	**264**	96	461	264	**462**	**263**	462	263
508.namd_r	96	400	228	**402**	**227**	409	223	96	403	226	**400**	**228**	400	228
510.parest_r	96	1056	238	1070	235	**1066**	**236**	96	1067	235	**1062**	**237**	1060	237
511.povray_r	96	620	362	615	365	**617**	**363**	96	**528**	**425**	526	426	540	415
519.lbm_r	96	510	198	**510**	**198**	512	198	96	479	211	478	212	**479**	**211**
521.wrf_r	96	546	394	553	389	**546**	**394**	96	**542**	**396**	537	401	556	387
526.blender_r	96	**442**	**331**	442	331	442	331	96	450	325	**450**	**325**	449	325
527.cam4_r	96	510	329	**508**	**330**	508	331	96	507	331	510	329	**509**	**330**
538.imagick_r	96	485	492	484	493	**485**	**493**	96	**484**	**493**	485	493	484	493
544.nab_r	96	**377**	**428**	378	428	376	430	96	**366**	**441**	366	441	366	441
549.fotonik3d_r	96	**1397**	**268**	1397	268	1400	267	96	**1397**	**268**	1397	268	1398	268
554.roms_r	96	798	191	792	193	**793**	**192**	96	779	196	**778**	**196**	777	196
SPECrate®2017_fp_base =		**325**										
SPECrate®2017_fp_peak =		**332**										

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /opt/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-qew3 Fri Oct 27 20:38:29 2017

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
       4  "physical id"s (chips)
       96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 12
       siblings  : 24
       physical 0: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 1: cores 0 1 3 9 10 16 18 19 24 25 26 27
       physical 2: cores 0 1 2 3 4 9 10 16 18 19 25 26
       physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26

  From lscpu:
       Architecture:          x86_64
       CPU op-mode(s):        32-bit, 64-bit
       Byte Order:            Little Endian
       CPU(s):                96
       On-line CPU(s) list:   0-95
       Thread(s) per core:    2
       Core(s) per socket:    12
       Socket(s):             4
       NUMA node(s):          8
       Vendor ID:             GenuineIntel
       CPU family:            6
       Model:                 85
       Model name:            Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
       Stepping:              4
       CPU MHz:               2262.399
       CPU max MHz:           3700.0000
       CPU min MHz:           1200.0000
       BogoMIPS:              6000.24
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```
        Virtualization:        VT-x
        L1d cache:             32K
        L1i cache:             32K
        L2 cache:              1024K
        L3 cache:              25344K
        NUMA node0 CPU(s):     0-2,5,7,10,48-50,53,55,58
        NUMA node1 CPU(s):     3,4,6,8,9,11,51,52,54,56,57,59
        NUMA node2 CPU(s):     12,13,15,17,20,21,60,61,63,65,68,69
        NUMA node3 CPU(s):     14,16,18,19,22,23,62,64,66,67,70,71
        NUMA node4 CPU(s):     24-26,29,31,34,72-74,77,79,82
        NUMA node5 CPU(s):     27,28,30,32,33,35,75,76,78,80,81,83
        NUMA node6 CPU(s):     36-38,41,43,46,84-86,89,91,94
        NUMA node7 CPU(s):     39,40,42,44,45,47,87,88,90,92,93,95
        Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
    hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnmi flexpriority ept vpid
    fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
    avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
    xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
   cache size : 25344 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 8 nodes (0-7)
   node 0 cpus: 0 1 2 5 7 10 48 49 50 53 55 58
   node 0 size: 95326 MB
   node 0 free: 94979 MB
   node 1 cpus: 3 4 6 8 9 11 51 52 54 56 57 59
   node 1 size: 96760 MB
   node 1 free: 96046 MB
   node 2 cpus: 12 13 15 17 20 21 60 61 63 65 68 69
   node 2 size: 96760 MB
   node 2 free: 96467 MB
   node 3 cpus: 14 16 18 19 22 23 62 64 66 67 70 71
   node 3 size: 96760 MB
   node 3 free: 96460 MB
   node 4 cpus: 24 25 26 29 31 34 72 73 74 77 79 82
   node 4 size: 96760 MB
   node 4 free: 96508 MB
   node 5 cpus: 27 28 30 32 33 35 75 76 78 80 81 83
   node 5 size: 96760 MB
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```
   node 5 free: 96484 MB
   node 6 cpus: 36 37 38 41 43 46 84 85 86 89 91 94
   node 6 size: 96760 MB
   node 6 free: 96406 MB
   node 7 cpus: 39 40 42 44 45 47 87 88 90 92 93 95
   node 7 size: 96757 MB
   node 7 free: 96465 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  31  31
     1:  11  10  21  21  21  21  31  31
     2:  21  21  10  11  31  31  21  21
     3:  21  21  11  10  31  31  21  21
     4:  21  21  31  31  10  11  21  21
     5:  21  21  31  31  11  10  21  21
     6:  31  31  21  21  21  21  10  11
     7:  31  31  21  21  21  21  11  10

 From /proc/meminfo
    MemTotal:       791190356 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 2
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP2"
       VERSION_ID="12.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
       ID="sles"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-qew3 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Oct 27 20:30

 SPEC is set to: /opt/cpu2017
    Filesystem      Type    Size   Used Avail Use% Mounted on
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019		**Test Date:**	Oct-2017
Test Sponsor: Cisco Systems		**Hardware Availability:** Aug-2017
Tested by: Cisco Systems		**Software Availability:** Sep-2017

Platform Notes (Continued)

```
     /dev/sdc1      btrfs 1.9T  121G  1.7T   7% /opt

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C480M5.3.1.0.272.0613172154 06/13/2017
   Memory:
    48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                  | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                   | 544.nab_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++                | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(base, peak) 526.blender_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.0 20170811
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019		**Test Date:**	Oct-2017
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Sep-2017

Compiler Version Notes (Continued)

```
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------


==========================================================================
Fortran        | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
               | 554.roms_r(base, peak)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------


==========================================================================
Fortran, C     | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
--------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Fortran benchmarks:
`ifort`

Benchmarks using both Fortran and C:
`ifort icc`

Benchmarks using both C and C++:
`icpc icc`

Benchmarks using Fortran, C, and C++:
`icpc icc ifort`

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License:	9019	**Test Date:**	Oct-2017
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Sep-2017

Base Portability Flags (Continued)

507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3`

C++ benchmarks:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs`
`-align array32byte`

Benchmarks using both Fortran and C:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs`
`-align array32byte`

Benchmarks using both C and C++:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch`
`-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs`
`-align array32byte`

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Base Other Flags

C benchmarks:
```
-m64 -std=c11
```

C++ benchmarks:
```
-m64
```

Fortran benchmarks:
```
-m64
```

Benchmarks using both Fortran and C:
```
-m64 -std=c11
```

Benchmarks using both C and C++:
```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
-m64 -std=c11
```

Peak Compiler Invocation

C benchmarks:
```
icc
```

C++ benchmarks:
```
icpc
```

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using both C and C++:
```
icpc icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Peak Optimization Flags

C benchmarks:

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r

C++ benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -mtune=skylake -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8158, 3.00GHz)

SPECrate®2017_fp_base = 325

SPECrate®2017_fp_peak = 332

Peak Other Flags

C benchmarks:
```
-m64 -std=c11
```

C++ benchmarks:
```
-m64
```

Fortran benchmarks:
```
-m64
```

Benchmarks using both Fortran and C:
```
-m64 -std=c11
```

Benchmarks using both C and C++:
```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
-m64 -std=c11
```

The flags files that were used to format this result can be browsed at
```
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html
```

You can also download the XML flags sources by saving the following links:
```
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml
```

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-10-27 23:38:28-0400.
Report generated on 2020-09-03 17:42:30 by CPU2017 PDF formatter v6255.
Originally published on 2017-11-14.