



SPEC CPU®2017 Floating Point Rate Result

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Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4110, 2.10 GHz)

SPECrate®2017_fp_base = 84.3

SPECrate®2017_fp_peak = 86.8

CPU2017 License: 9019

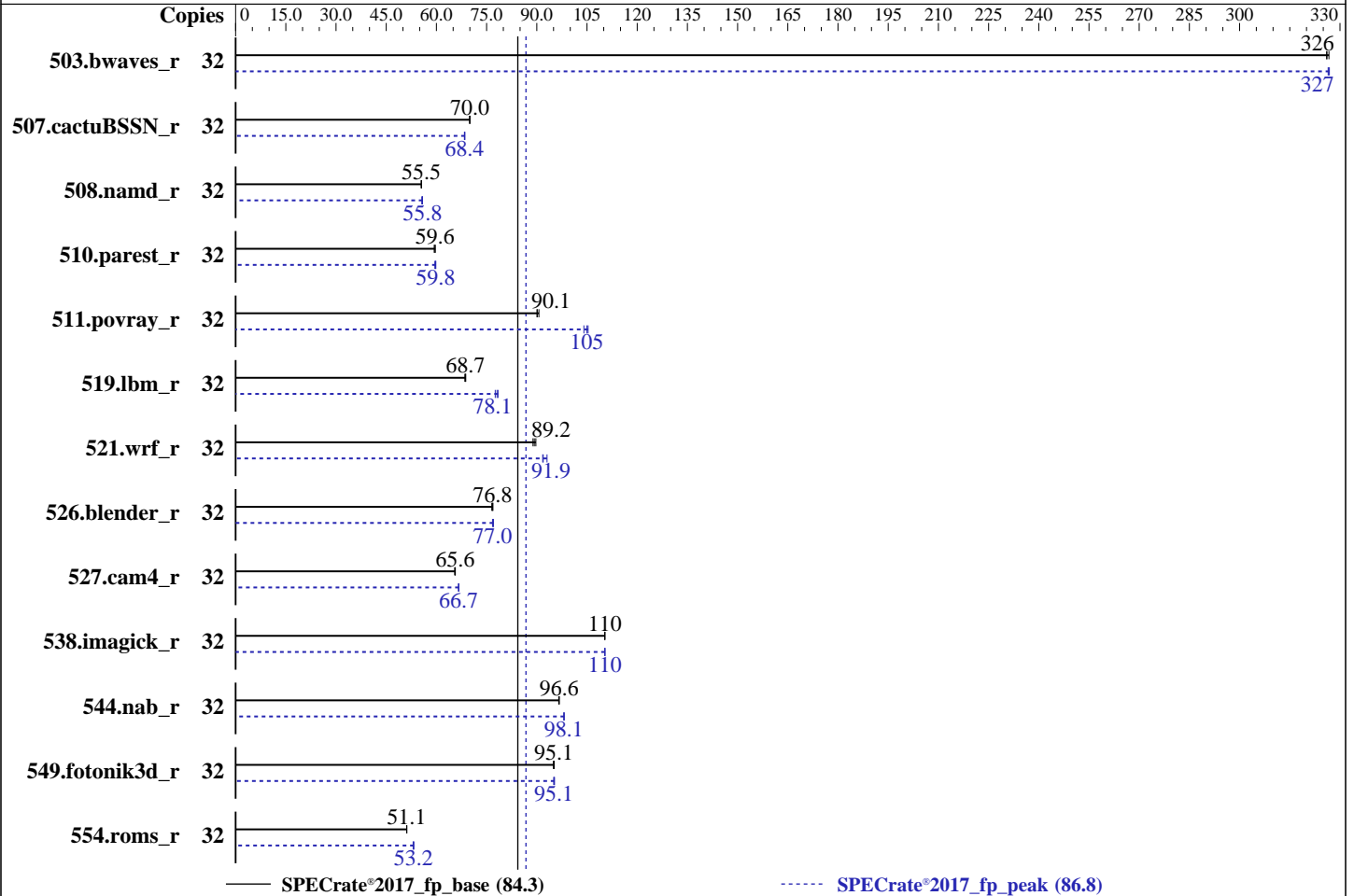
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2017

Hardware Availability: Aug-2017

Software Availability: Sep-2017



Hardware

CPU Name: Intel Xeon Silver 4110
 Max MHz: 3000
 Nominal: 2100
 Enabled: 16 cores, 2 chips, 2 threads/core
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 11 MB I+D on chip per chip
 Other: None
 Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
 Storage: 1 x 600 GB SAS HDD, 10K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 3.2.1d released Jul-2017
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: None
 Power Management: --



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Results Table

| Benchmark | Base | | | | | | | Peak | | | | | | |
|-----------------|--------|------------|-------------|-------------|-------------|-------------|-------------|--------|------------|-------------|-------------|-------------|------------|-------------|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 503.bwaves_r | 32 | 984 | 326 | 982 | 327 | 984 | 326 | 32 | 983 | 326 | 983 | 327 | 982 | 327 |
| 507.cactuBSSN_r | 32 | 579 | 69.9 | 579 | 70.0 | 579 | 70.0 | 32 | 591 | 68.5 | 593 | 68.4 | 592 | 68.4 |
| 508.namd_r | 32 | 548 | 55.5 | 548 | 55.4 | 547 | 55.6 | 32 | 547 | 55.6 | 544 | 55.8 | 544 | 55.9 |
| 510.parest_r | 32 | 1403 | 59.7 | 1406 | 59.6 | 1411 | 59.3 | 32 | 1406 | 59.5 | 1401 | 59.8 | 1399 | 59.8 |
| 511.povray_r | 32 | 829 | 90.1 | 829 | 90.1 | 824 | 90.6 | 32 | 718 | 104 | 709 | 105 | 712 | 105 |
| 519.lbm_r | 32 | 492 | 68.5 | 490 | 68.8 | 491 | 68.7 | 32 | 432 | 78.1 | 435 | 77.6 | 430 | 78.4 |
| 521.wrf_r | 32 | 803 | 89.2 | 807 | 88.9 | 799 | 89.7 | 32 | 770 | 93.1 | 781 | 91.8 | 780 | 91.9 |
| 526.blender_r | 32 | 637 | 76.5 | 634 | 76.9 | 634 | 76.8 | 32 | 633 | 77.0 | 633 | 77.0 | 635 | 76.8 |
| 527.cam4_r | 32 | 855 | 65.4 | 853 | 65.6 | 853 | 65.6 | 32 | 841 | 66.6 | 839 | 66.7 | 840 | 66.7 |
| 538.imagick_r | 32 | 721 | 110 | 721 | 110 | 721 | 110 | 32 | 721 | 110 | 721 | 110 | 721 | 110 |
| 544.nab_r | 32 | 557 | 96.6 | 558 | 96.6 | 557 | 96.7 | 32 | 548 | 98.2 | 549 | 98.1 | 549 | 98.1 |
| 549.fotonik3d_r | 32 | 1310 | 95.2 | 1314 | 94.9 | 1311 | 95.1 | 32 | 1309 | 95.3 | 1311 | 95.1 | 1312 | 95.1 |
| 554.roms_r | 32 | 995 | 51.1 | 994 | 51.1 | 994 | 51.2 | 32 | 955 | 53.3 | 956 | 53.2 | 959 | 53.0 |

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```



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Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

running on linux-qc7k Sun Nov 26 00:06:58 2017

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz

2 "physical id"s (chips)

32 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 8

siblings : 16

physical 0: cores 0 1 2 3 4 5 6 7

physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 32

On-line CPU(s) list: 0-31

Thread(s) per core: 2

Core(s) per socket: 8

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

Model name: Intel(R) Xeon(R) Silver 4110 CPU @ 2.10GHz

Stepping: 4

CPU MHz: 1073.721

CPU max MHz: 3000.0000

CPU min MHz: 800.0000

BogoMIPS: 4200.00

Virtualization: VT-x

L1d cache: 32K

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Platform Notes (Continued)

```

L1i cache:          32K
L2 cache:           1024K
L3 cache:           11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vnmi flexpriority ept vpid
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

```

```
/proc/cpuinfo cache data
cache size : 11264 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 192830 MB
node 0 free: 192109 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 193504 MB
node 1 free: 192835 MB
node distances:
node    0    1
 0:   10   21
 1:   21   10

```

```

From /proc/meminfo
MemTotal:          395606536 kB
HugePages_Total:      0
Hugepagesize:       2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"

```

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Platform Notes (Continued)

```
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-qc7k 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 31 19:32
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   224G   38G  187G  17% /
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666, configured at 2400
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
-----
```

```
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

```
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C    | 511.povray_r(base, peak) 526.blender_r(base, peak)
-----
```

(Continued on next page)



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Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

=====
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

C++ benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

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Base Optimization Flags (Continued)

Benchmarks using both C and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Base Other Flags

C benchmarks:

```
-m64 -std=c11
```

C++ benchmarks:

```
-m64
```

Fortran benchmarks:

```
-m64
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11
```

Benchmarks using both C and C++:

```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11
```

Peak Compiler Invocation

C benchmarks:

```
icc
```

C++ benchmarks:

```
icpc
```

Fortran benchmarks:

```
ifort
```

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Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using both C and C++:

icpc icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 519.lbm_r

C++ benchmarks:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs

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Peak Optimization Flags (Continued)

554.roms_r (continued):

-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

Benchmarks using Fortran, C, and C++:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte

Peak Other Flags

C benchmarks:

-m64 -std=c11

C++ benchmarks:

-m64

Fortran benchmarks:

-m64

Benchmarks using both Fortran and C:

-m64 -std=c11

Benchmarks using both C and C++:

-m64 -std=c11

Benchmarks using Fortran, C, and C++:

-m64 -std=c11

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>



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You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2017-11-26 00:06:58-0500.

Report generated on 2020-06-25 18:24:50 by CPU2017 PDF formatter v6255.

Originally published on 2017-12-26.