



# SPEC® CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

CPU2017 License: 9019

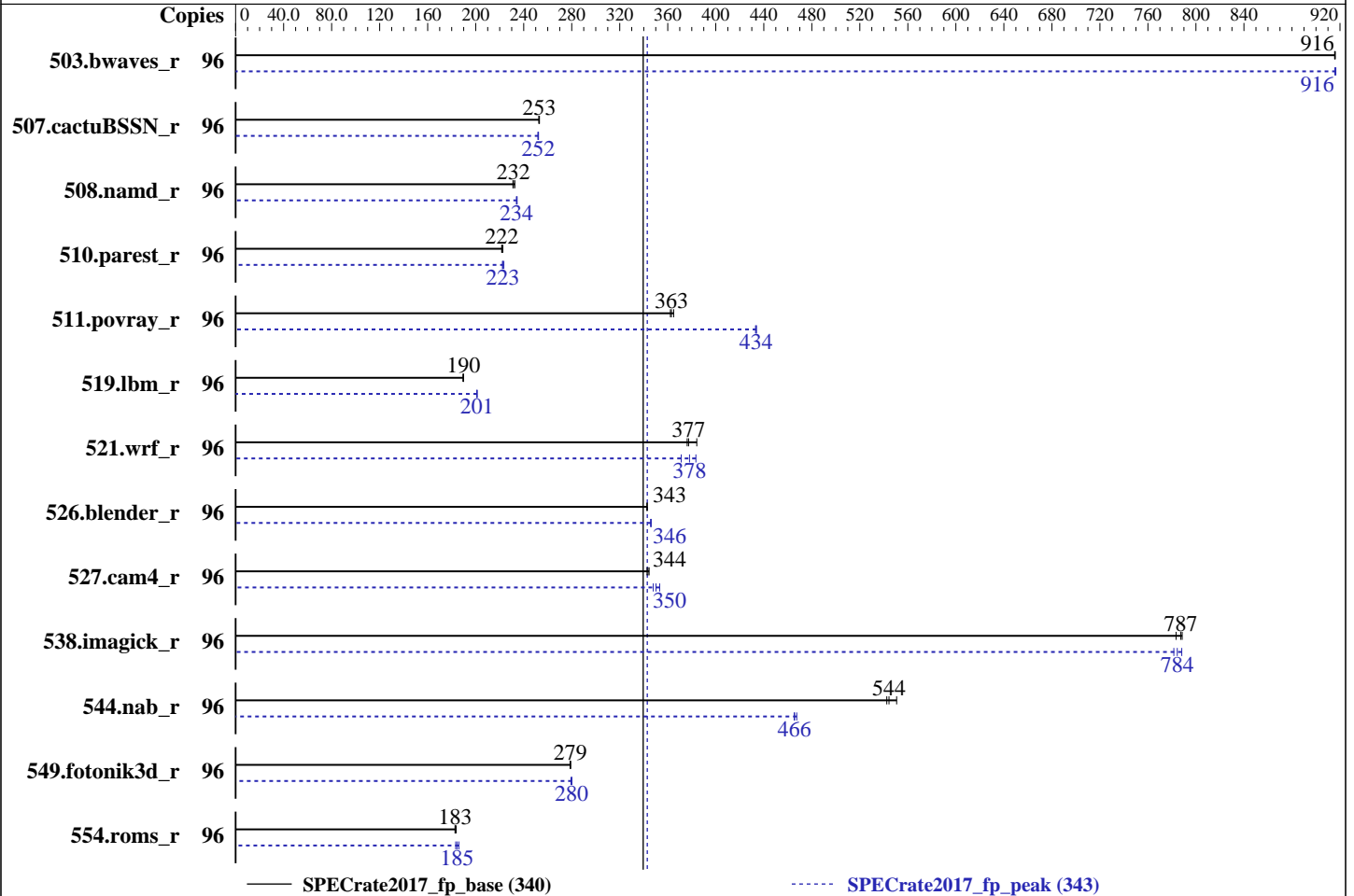
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018



### Hardware

CPU Name: Intel Xeon Platinum 8158  
 Max MHz.: 3700  
 Nominal: 3000  
 Enabled: 48 cores, 4 chips, 2 threads/core  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)  
 Storage: 1 x 400 GB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64) 4.4.120-92.70-default  
 Compiler: C/C++: Version 18.0.2.199 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 18.0.2.199 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 3.2.3c released Mar-2018  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	96	1051	916	<b>1051</b>	<b>916</b>	1051	916	96	<b>1051</b>	<b>916</b>	1050	917	1051	916
507.cactuBSSN_r	96	481	253	<b>480</b>	<b>253</b>	480	253	96	482	252	483	252	<b>482</b>	<b>252</b>
508.namd_r	96	395	231	<b>394</b>	<b>232</b>	392	233	96	390	234	<b>390</b>	<b>234</b>	389	235
510.parest_r	96	1128	223	1133	222	<b>1132</b>	<b>222</b>	96	1124	223	<b>1129</b>	<b>223</b>	1130	222
511.povray_r	96	<b>617</b>	<b>363</b>	619	362	614	365	96	518	433	517	434	<b>517</b>	<b>434</b>
519.lbm_r	96	534	189	533	190	<b>533</b>	<b>190</b>	96	503	201	504	201	<b>503</b>	<b>201</b>
521.wrf_r	96	572	376	560	384	<b>570</b>	<b>377</b>	96	561	383	<b>569</b>	<b>378</b>	579	371
526.blender_r	96	427	343	<b>427</b>	<b>343</b>	427	343	96	422	346	423	346	<b>423</b>	<b>346</b>
527.cam4_r	96	487	344	490	343	<b>489</b>	<b>344</b>	96	483	348	475	353	<b>479</b>	<b>350</b>
538.imagick_r	96	303	789	305	783	<b>303</b>	<b>787</b>	96	<b>304</b>	<b>784</b>	305	782	303	788
544.nab_r	96	<b>297</b>	<b>544</b>	298	542	293	551	96	<b>347</b>	<b>466</b>	347	465	346	467
549.fotonik3d_r	96	1340	279	1342	279	<b>1342</b>	<b>279</b>	96	1339	279	1336	280	<b>1336</b>	<b>280</b>
554.roms_r	96	830	184	<b>834</b>	<b>183</b>	834	183	96	<b>827</b>	<b>185</b>	832	183	820	186

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.4  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

    Sysinfo program /home/cpu2017/bin/sysinfo  
    Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
    running on linux-xy4f Mon Nov 19 22:22:03 2018

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

    model name : Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz

    4 "physical id"s (chips)

    96 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

    cpu cores : 12

    siblings : 24

    physical 0: cores 0 1 2 3 4 9 10 16 18 19 25 26

    physical 1: cores 0 1 2 3 4 9 10 16 18 19 25 26

    physical 2: cores 0 1 3 9 10 16 18 19 24 25 26 27

    physical 3: cores 0 1 2 3 4 9 10 16 18 19 25 26

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 96

On-line CPU(s) list: 0-95

Thread(s) per core: 2

Core(s) per socket: 12

Socket(s): 4

NUMA node(s): 8

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Platform Notes (Continued)

```

Vendor ID:           GenuineIntel
CPU family:         6
Model:              85
Model name:         Intel(R) Xeon(R) Platinum 8158 CPU @ 3.00GHz
Stepping:           4
CPU MHz:            1209.543
CPU max MHz:        3700.0000
CPU min MHz:        1200.0000
BogoMIPS:           5999.99
Virtualization:     VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           25344K
NUMA node0 CPU(s): 0-2,5,7,10,48-50,53,55,58
NUMA node1 CPU(s): 3,4,6,8,9,11,51,52,54,56,57,59
NUMA node2 CPU(s): 12-14,17,19,22,60-62,65,67,70
NUMA node3 CPU(s): 15,16,18,20,21,23,63,64,66,68,69,71
NUMA node4 CPU(s): 24,25,27,29,32,33,72,73,75,77,80,81
NUMA node5 CPU(s): 26,28,30,31,34,35,74,76,78,79,82,83
NUMA node6 CPU(s): 36-38,41,43,46,84-86,89,91,94
NUMA node7 CPU(s): 39,40,42,44,45,47,87,88,90,92,93,95
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx fl16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```
/proc/cpuinfo cache data
cache size : 25344 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 8 nodes (0-7)
node 0 cpus: 0 1 2 5 7 10 48 49 50 53 55 58
node 0 size: 192095 MB
node 0 free: 191937 MB
node 1 cpus: 3 4 6 8 9 11 51 52 54 56 57 59
node 1 size: 193528 MB
node 1 free: 193385 MB
node 2 cpus: 12 13 14 17 19 22 60 61 62 65 67 70
node 2 size: 193528 MB

```

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

### Platform Notes (Continued)

```

node 2 free: 193397 MB
node 3 cpus: 15 16 18 20 21 23 63 64 66 68 69 71
node 3 size: 193528 MB
node 3 free: 193388 MB
node 4 cpus: 24 25 27 29 32 33 72 73 75 77 80 81
node 4 size: 193528 MB
node 4 free: 193361 MB
node 5 cpus: 26 28 30 31 34 35 74 76 78 79 82 83
node 5 size: 193528 MB
node 5 free: 193397 MB
node 6 cpus: 36 37 38 41 43 46 84 85 86 89 91 94
node 6 size: 193528 MB
node 6 free: 193391 MB
node 7 cpus: 39 40 42 44 45 47 87 88 90 92 93 95
node 7 size: 193525 MB
node 7 free: 193389 MB
node distances:
node  0  1  2  3  4  5  6  7
  0: 10 11 21 21 21 21 21 21
  1: 11 10 21 21 21 21 21 21
  2: 21 21 10 11 21 21 21 21
  3: 21 21 11 10 21 21 21 21
  4: 21 21 21 21 10 11 21 21
  5: 21 21 21 21 11 10 21 21
  6: 21 21 21 21 21 21 10 11
  7: 21 21 21 21 21 21 11 10

```

From /proc/meminfo

```

MemTotal:      1583915000 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/\*release\* /etc/\*version\*

SuSE-release:

```

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2

```

```

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

```

os-release:

```

NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

### Platform Notes (Continued)

```

uname -a:
Linux linux-xy4f 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 00:23

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   224G   70G  154G  32% /

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B480M5.3.2.3c.0.0307181316 03/07/2018
Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

```

### Compiler Version Notes

```

=====
CC 519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base)
-----

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

=====
CC 519.lbm_r(peak) 544.nab_r(peak)
-----

icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

=====
CXXC 508.namd_r(base) 510.parest_r(base)
-----

icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----

=====
CXXC 508.namd_r(peak) 510.parest_r(peak)
-----

```

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Nov-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Mar-2018

### Compiler Version Notes (Continued)

-----  
icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
CC 511.povray\_r(base) 526.blender\_r(base)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
CC 511.povray\_r(peak) 526.blender\_r(peak)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
FC 507.cactuBSSN\_r(base)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
FC 507.cactuBSSN\_r(peak)  
-----

icpc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
icc (ICC) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
ifort (IFORT) 18.0.2 20180210  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

=====  
FC 503.bwaves\_r(base, peak) 549.fotonik3d\_r(base, peak) 554.roms\_r(base)  
-----

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Compiler Version Notes (Continued)

```
-----
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
```

```
=====
FC 554.roms_r(peak)
-----
```

```
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
```

```
=====
CC 521.wrf_r(base) 527.cam4_r(base)
-----
```

```
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
```

```
=====
CC 521.wrf_r(peak) 527.cam4_r(peak)
-----
```

```
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
-----
```

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

(Continued on next page)





# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Platinum 8158,  
3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

```
538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

(Continued on next page)



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158, 3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

## Peak Optimization Flags (Continued)

544.nab\_r: Same as 519.lbm\_r

C++ benchmarks:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d\_r: Same as 503.bwaves\_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>



# SPEC CPU2017 Floating Point Rate Result

Copyright 2017-2018 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8158,  
3.00 GHz)

SPECrate2017\_fp\_base = 340

SPECrate2017\_fp\_peak = 343

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Nov-2018

**Hardware Availability:** Aug-2017

**Software Availability:** Mar-2018

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU2017 v1.0.2 on 2018-11-19 22:22:02-0500.

Report generated on 2018-12-11 15:02:12 by CPU2017 PDF formatter v6067.

Originally published on 2018-12-11.