SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

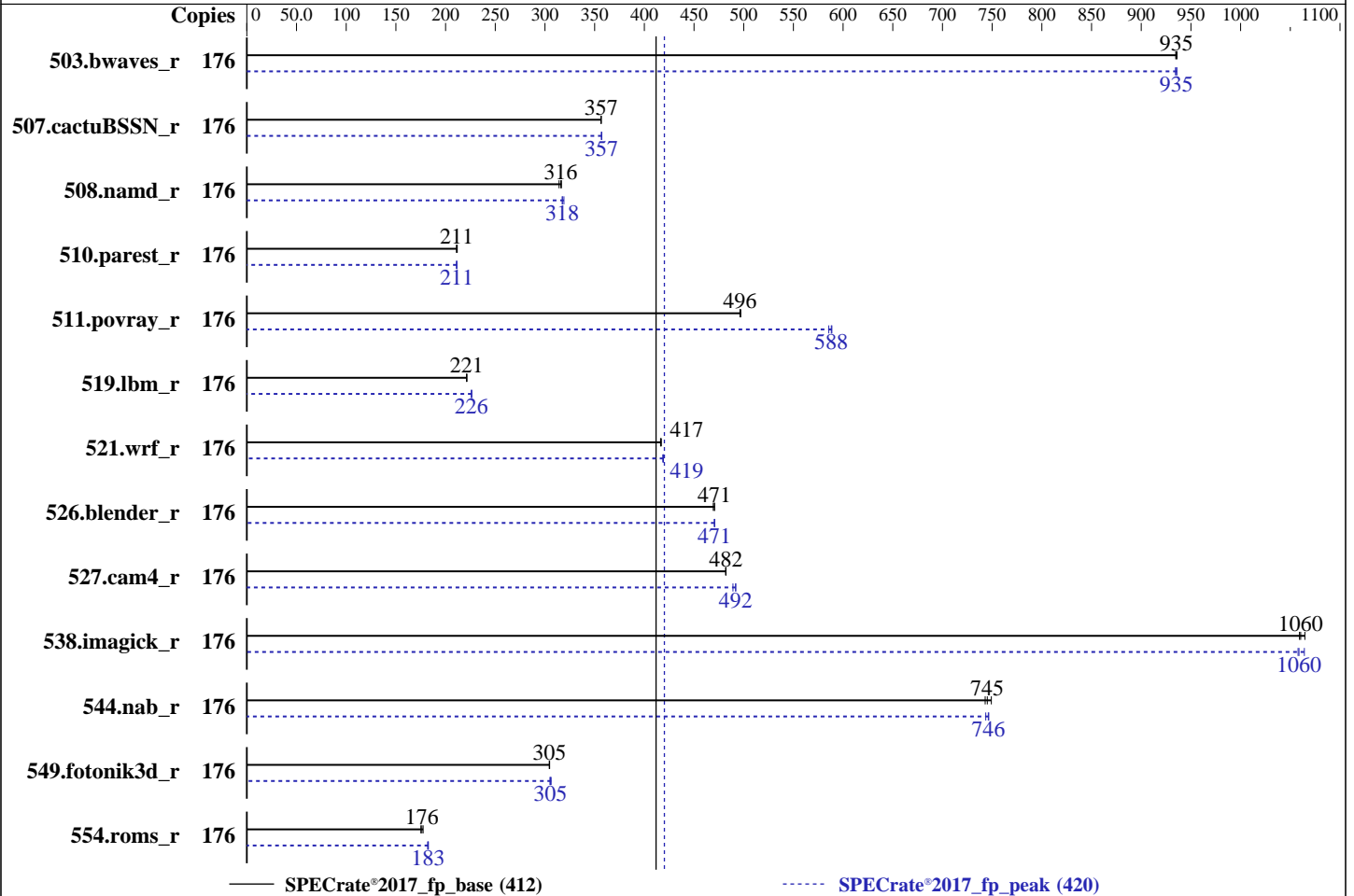SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Benchmark	Copies	base	peak
503.bwaves_r	176	935	935
507.cactuBSSN_r	176	357	357
508.namd_r	176	316	318
510.parest_r	176	211	211
511.povray_r	176	496	588
519.lbm_r	176	221	226
521.wrf_r	176	417	419
526.blender_r	176	471	471
527.cam4_r	176	482	492
538.imagick_r	176	1060	1060
544.nab_r	176	745	746
549.fotonik3d_r	176	305	305
554.roms_r	176	176	183

SPECrate®2017_fp_base (412)

SPECrate®2017_fp_peak (420)

Hardware

CPU Name: Intel Xeon Gold 6152
  Max MHz: 3700
  Nominal: 2100
Enabled: 88 cores, 4 chips, 2 threads/core
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
  L2: 1 MB I+D on chip per core
  L3: 30.25 MB I+D on chip per chip
  Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 1 TB HDD, 7.2K RPM
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64)
4.4.120-92.70-default
Compiler: C/C++: Version 18.0.2.199 of Intel C/C++
Compiler for Linux;
Fortran: Version 18.0.2.199 of Intel Fortran
Compiler for Linux
Parallel: No
Firmware: Version 3.1.3e released Jun-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	176	**1887**	**935**	1886	936	1888	935	176	1886	936	**1887**	**935**	1889	934
507.cactuBSSN_r	176	625	357	625	356	**625**	**357**	176	624	357	624	357	**624**	**357**
508.namd_r	176	532	314	528	317	**529**	**316**	176	524	319	527	317	**527**	**318**
510.parest_r	176	**2180**	**211**	2182	211	2174	212	176	**2180**	**211**	2179	211	2182	211
511.povray_r	176	**828**	**496**	828	496	827	497	176	698	589	**699**	**588**	702	586
519.lbm_r	176	838	221	838	221	**838**	**221**	176	**821**	**226**	820	226	821	226
521.wrf_r	176	947	416	**947**	**417**	945	417	176	**941**	**419**	942	419	940	419
526.blender_r	176	**570**	**471**	571	469	570	471	176	570	471	569	471	**570**	**471**
527.cam4_r	176	638	482	639	482	**639**	**482**	176	**626**	**492**	626	492	629	489
538.imagick_r	176	413	1060	**413**	**1060**	411	1060	176	414	1060	**413**	**1060**	411	1060
544.nab_r	176	395	749	**398**	**745**	399	743	176	398	744	397	747	**397**	**746**
549.fotonik3d_r	176	2253	304	**2252**	**305**	2251	305	176	**2245**	**305**	2240	306	2248	305
554.roms_r	176	1597	175	**1588**	**176**	1577	177	176	**1532**	**183**	1537	182	1531	183

SPECrate®2017_fp_base =	**412**
SPECrate®2017_fp_peak =	**420**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-6700K CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
 running on linux-9r4j Thu Nov 15 18:54:03 2018

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
       4  "physical id"s (chips)
       176 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 22
       siblings  : 44
       physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
       physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

  From lscpu:
       Architecture:          x86_64
       CPU op-mode(s):        32-bit, 64-bit
       Byte Order:            Little Endian
       CPU(s):                176
       On-line CPU(s) list:   0-175
       Thread(s) per core:    2
       Core(s) per socket:    22
       Socket(s):             4
       NUMA node(s):          8
       Vendor ID:             GenuineIntel
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152
2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2018

Hardware Availability: Aug-2017

Software Availability: Mar-2018

Platform Notes (Continued)

```
        CPU family:            6
        Model:                 85
        Model name:            Intel(R) Xeon(R) Gold 6152 CPU @ 2.10GHz
        Stepping:              4
        CPU MHz:               2411.870
        CPU max MHz:           3700.0000
        CPU min MHz:           1000.0000
        BogoMIPS:              4195.47
        Virtualization:        VT-x
        L1d cache:             32K
        L1i cache:             32K
        L2 cache:              1024K
        L3 cache:              30976K
        NUMA node0 CPU(s):     0-2,6-8,11-13,17,18,88-90,94-96,99-101,105,106
        NUMA node1 CPU(s):     3-5,9,10,14-16,19-21,91-93,97,98,102-104,107-109
        NUMA node2 CPU(s):     22-24,28-30,33-35,39,40,110-112,116-118,121-123,127,128
        NUMA node3 CPU(s):     25-27,31,32,36-38,41-43,113-115,119,120,124-126,129-131
        NUMA node4 CPU(s):     44-46,50-52,55-57,61,62,132-134,138-140,143-145,149,150
        NUMA node5 CPU(s):     47-49,53,54,58-60,63-65,135-137,141,142,146-148,151-153
        NUMA node6 CPU(s):     66-68,72-74,77-79,83,84,154-156,160-162,165-167,171,172
        NUMA node7 CPU(s):     69-71,75,76,80-82,85-87,157-159,163,164,168-170,173-175
        Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
    dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
    retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
    avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
    clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

  /proc/cpuinfo cache data
     cache size : 30976 KB

  From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
    available: 8 nodes (0-7)
    node 0 cpus: 0 1 2 6 7 8 11 12 13 17 18 88 89 90 94 95 96 99 100 101 105 106
    node 0 size: 192094 MB
    node 0 free: 191906 MB
    node 1 cpus: 3 4 5 9 10 14 15 16 19 20 21 91 92 93 97 98 102 103 104 107 108 109
    node 1 size: 193528 MB
    node 1 free: 193301 MB
    node 2 cpus: 22 23 24 28 29 30 33 34 35 39 40 110 111 112 116 117 118 121 122 123 127
    128
    node 2 size: 193528 MB
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Platform Notes (Continued)

```
   node 2 free: 193362 MB
   node 3 cpus: 25 26 27 31 32 36 37 38 41 42 43 113 114 115 119 120 124 125 126 129 130
   131
   node 3 size: 193528 MB
   node 3 free: 193224 MB
   node 4 cpus: 44 45 46 50 51 52 55 56 57 61 62 132 133 134 138 139 140 143 144 145 149
   150
   node 4 size: 193528 MB
   node 4 free: 193365 MB
   node 5 cpus: 47 48 49 53 54 58 59 60 63 64 65 135 136 137 141 142 146 147 148 151 152
   153
   node 5 size: 193528 MB
   node 5 free: 193350 MB
   node 6 cpus: 66 67 68 72 73 74 77 78 79 83 84 154 155 156 160 161 162 165 166 167 171
   172
   node 6 size: 193528 MB
   node 6 free: 193369 MB
   node 7 cpus: 69 70 71 75 76 80 81 82 85 86 87 157 158 159 163 164 168 169 170 173 174
   175
   node 7 size: 193525 MB
   node 7 free: 193362 MB
   node distances:
   node   0   1   2   3   4   5   6   7
     0:  10  11  21  21  21  21  21  21
     1:  11  10  21  21  21  21  21  21
     2:  21  21  10  11  21  21  21  21
     3:  21  21  11  10  21  21  21  21
     4:  21  21  21  21  10  11  21  21
     5:  21  21  21  21  11  10  21  21
     6:  21  21  21  21  21  21  10  11
     7:  21  21  21  21  21  21  11  10

 From /proc/meminfo
    MemTotal:       1583914404 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 2
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP2"
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License:	9019	**Test Date:**	Nov-2018
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Aug-2017
Tested by:	Cisco Systems	**Software Availability:**	Mar-2018

Platform Notes (Continued)

```
        VERSION_ID="12.2"
        PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
        ID="sles"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

 uname -a:
    Linux linux-9r4j 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

 run-level 3 Nov 15 18:44

 SPEC is set to: /home/cpu2017
    Filesystem     Type  Size  Used Avail Use% Mounted on
    /dev/sda1      xfs   930G  244G  687G  27% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018
   Memory:
    48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                  | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                   | 544.nab_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++                | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(base, peak) 526.blender_r(base, peak)
------------------------------------------------------------------------------
```

(Continued on next page)

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Compiler Version Notes (Continued)

```
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                | 554.roms_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.2 20180210
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

C++ benchmarks:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Fortran benchmarks:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Peak Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Benchmarks using both Fortran and C:
```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

Peak Optimization Flags (Continued)

519.lbm_r (continued):
```
-qopt-mem-layout-trans=3
```

538.imagick_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

544.nab_r: `Same as 538.imagick_r`

C++ benchmarks:

508.namd_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

510.parest_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Fortran benchmarks:

503.bwaves_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

549.fotonik3d_r: `Same as 503.bwaves_r`

554.roms_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:
```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Benchmarks using both C and C++:

511.povray_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

526.blender_r: `-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

Benchmarks using Fortran, C, and C++:
```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
```

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6152 2.10 GHz)

SPECrate®2017_fp_base = 412

SPECrate®2017_fp_peak = 420

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2018
Hardware Availability: Aug-2017
Software Availability: Mar-2018

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2017-12-21.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-11-15 18:54:02-0500.
Report generated on 2020-08-04 14:49:43 by CPU2017 PDF formatter v6255.
Originally published on 2018-12-11.