



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPECrate®2017_fp_base = 197

SPECrate®2017_fp_peak = 202

CPU2017 License: 9019

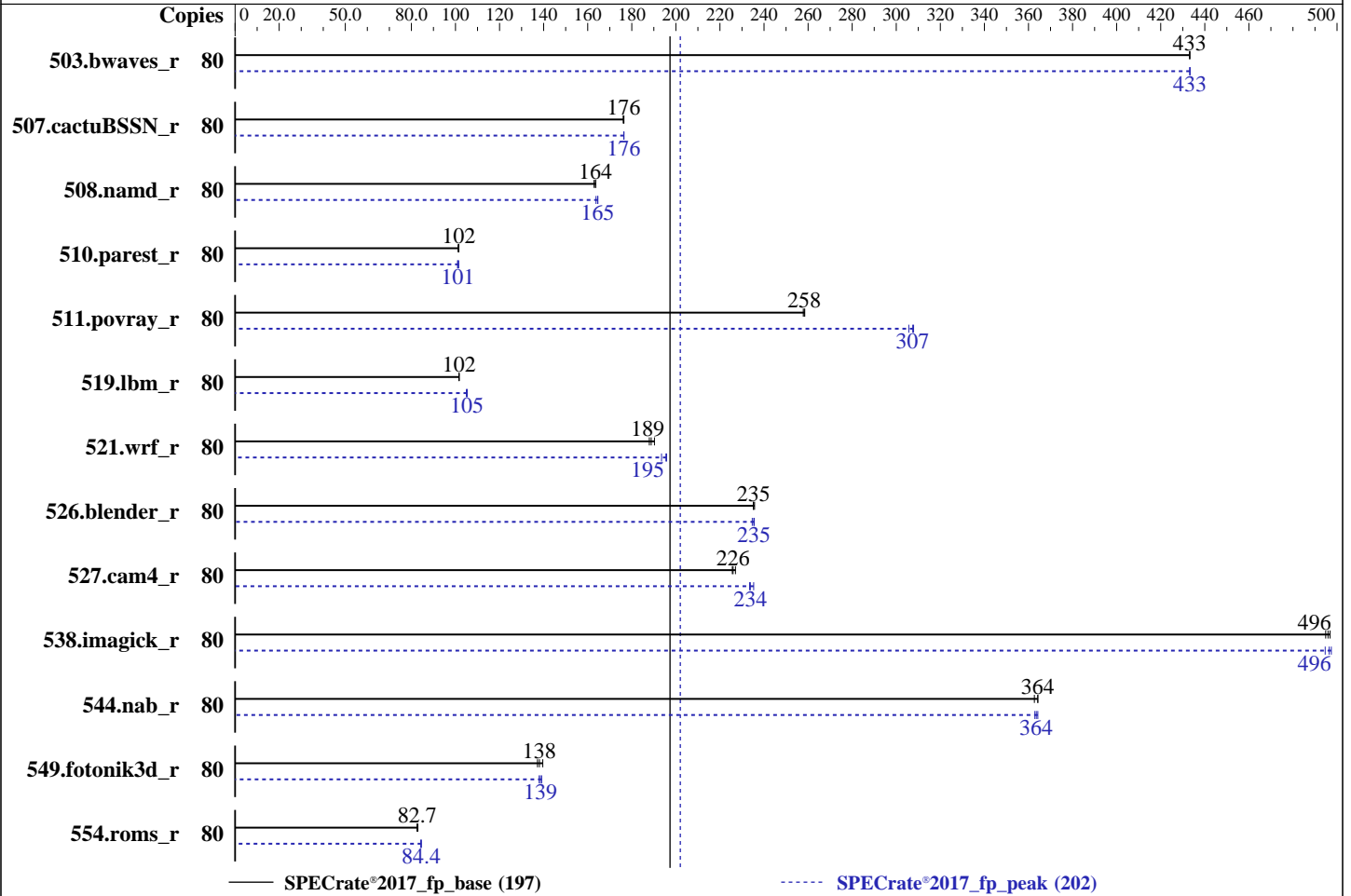
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2019

Hardware Availability: Aug-2017

Software Availability: Oct-2018



Hardware

CPU Name: Intel Xeon Gold 5115
 Max MHz: 3200
 Nominal: 2400
 Enabled: 40 cores, 4 chips, 2 threads/core
 Orderable: 2,4 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 13.75 MB I+D on chip per chip
 Other: None
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
 Storage: 1 x 1 TB HDD, 7.2K RPM
 Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default
 Compiler: C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 3.1.3e released Jun-2018
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: None
 Power Management: --



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	80	1852	433	1852	433	1852	433	80	1852	433	1852	433	1852	433
507.cactuBSSN_r	80	574	176	575	176	574	176	80	574	176	574	176	574	176
508.namd_r	80	465	164	465	164	467	163	80	462	165	464	164	462	165
510.parest_r	80	2061	102	2069	101	2062	102	80	2073	101	2062	101	2070	101
511.povray_r	80	723	258	725	258	723	258	80	607	308	608	307	611	306
519.lbm_r	80	830	102	829	102	829	102	80	802	105	803	105	801	105
521.wrf_r	80	953	188	949	189	942	190	80	915	196	926	193	917	195
526.blender_r	80	518	235	518	235	517	236	80	518	235	519	235	517	236
527.cam4_r	80	619	226	616	227	620	226	80	599	233	598	234	595	235
538.imagick_r	80	400	497	401	496	402	495	80	401	496	400	497	402	495
544.nab_r	80	370	364	371	363	370	364	80	370	364	371	363	370	364
549.fotonik3d_r	80	2272	137	2258	138	2233	140	80	2260	138	2250	139	2241	139
554.roms_r	80	1540	82.6	1538	82.7	1532	83.0	80	1506	84.4	1509	84.3	1504	84.5

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation

Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

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General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-e8np Sat Feb 16 03:14:57 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
 4 "physical id"s (chips)
 80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings  : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
physical 2: cores 0 1 2 3 4 8 9 10 11 12
physical 3: cores 0 1 2 3 4 8 9 10 11 12
```

```
From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 80
On-line CPU(s) list:   0-79
Thread(s) per core:    2
Core(s) per socket:    10
Socket(s):              4
NUMA node(s):          4
Vendor ID:              GenuineIntel
```

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Platform Notes (Continued)

```

CPU family:           6
Model:                85
Model name:           Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
Stepping:             4
CPU MHz:              2595.783
CPU max MHz:          3200.0000
CPU min MHz:          1000.0000
BogoMIPS:             4794.85
Virtualization:       VT-x
L1d cache:            32K
L1i cache:            32K
L2 cache:             1024K
L3 cache:             14080K
NUMA node0 CPU(s):   0-9,40-49
NUMA node1 CPU(s):   10-19,50-59
NUMA node2 CPU(s):   20-29,60-69
NUMA node3 CPU(s):   30-39,70-79

```

```

Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 14080 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
node 0 size: 386567 MB
node 0 free: 386301 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
node 1 size: 387057 MB
node 1 free: 386781 MB
node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
node 2 size: 387057 MB
node 2 free: 386701 MB
node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
node 3 size: 387054 MB
node 3 free: 386811 MB
node distances:

```

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Platform Notes (Continued)

node	0	1	2	3
0:	10	21	21	31
1:	21	10	31	21
2:	21	31	10	21
3:	31	21	21	10

From /proc/meminfo

MemTotal: 1584882180 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
This file is deprecated and will be removed in a future service pack or release.
Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Feb 16 03:07

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdal	xfs	894G	164G	730G	19%	/

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613181101 06/13/2018

Memory:

48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)



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Compiler Version Notes

```
=====
C                | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                  | 544.nab_r(base, peak)
=====
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====
```

```
=====
C++              | 508.namd_r(base, peak) 510.parest_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
=====
```

```
=====
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                  | 554.roms_r(base, peak)
=====
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```

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Compiler Version Notes (Continued)

64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.0.117 Build 20180804
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64

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Base Portability Flags (Continued)

```

521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

```

Base Optimization Flags

C benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

C++ benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

Fortran benchmarks:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
-align array32byte

```

Benchmarks using both Fortran and C:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
-align array32byte

```

Benchmarks using both C and C++:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

```

Benchmarks using Fortran, C, and C++:

```

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs
-align array32byte

```

Peak Compiler Invocation

C benchmarks:

```

icc -m64 -std=c11

```

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Peak Compiler Invocation (Continued)

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3

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Peak Optimization Flags (Continued)

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3 -auto  
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d_r: Same as 503.bwaves_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs  
-align array32byte
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs  
-align array32byte
```

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3
```

```
526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=3 -auto -nostandard-realloc-lhs  
-align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.html>
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.2019-01-15.xml>
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>



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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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