



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

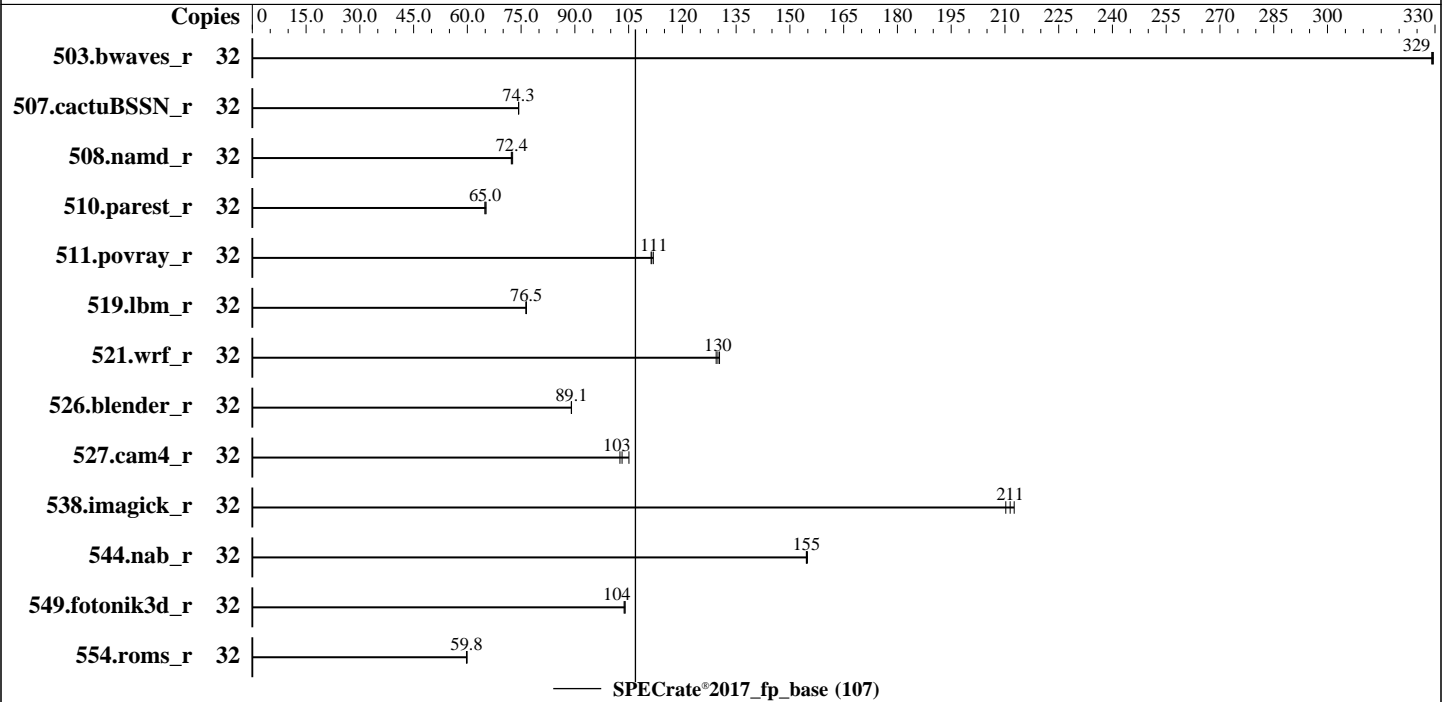
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2019

Hardware Availability: Apr-2019

Software Availability: Nov-2018



Hardware

CPU Name: Intel Xeon Silver 4215
 Max MHz: 3500
 Nominal: 2500
 Enabled: 16 cores, 2 chips, 2 threads/core
 Orderable: 1,2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 11 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
 Storage: 1 x 400 GB SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
 Compiler: C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux
 Parallel: No
 Firmware: Version 4.0.2.193 released Dec-2018
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: None
 Power Management: --



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Results Table

| Benchmark | Base | | | | | | | Peak | | | | | | |
|-----------------|--------|--------------------|--------------------|--------------------|--------------------|-------------------|--------------------|--------|---------|-------|---------|-------|---------|-------|
| | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio | Copies | Seconds | Ratio | Seconds | Ratio | Seconds | Ratio |
| 503.bwaves_r | 32 | 974 | 330 | <u>974</u> | <u>329</u> | 975 | 329 | | | | | | | |
| 507.cactuBSSN_r | 32 | 545 | 74.3 | <u>545</u> | <u>74.3</u> | 545 | 74.3 | | | | | | | |
| 508.namd_r | 32 | 421 | 72.3 | 419 | 72.6 | <u>420</u> | <u>72.4</u> | | | | | | | |
| 510.parest_r | 32 | 1283 | 65.2 | <u>1289</u> | <u>65.0</u> | 1289 | 64.9 | | | | | | | |
| 511.povray_r | 32 | <u>670</u> | <u>111</u> | 668 | 112 | 672 | 111 | | | | | | | |
| 519.lbm_r | 32 | 441 | 76.5 | <u>441</u> | <u>76.5</u> | 442 | 76.3 | | | | | | | |
| 521.wrf_r | 32 | 554 | 129 | 550 | 130 | <u>552</u> | <u>130</u> | | | | | | | |
| 526.blender_r | 32 | <u>547</u> | <u>89.1</u> | 548 | 89.0 | 547 | 89.1 | | | | | | | |
| 527.cam4_r | 32 | 533 | 105 | <u>543</u> | <u>103</u> | 546 | 103 | | | | | | | |
| 538.imagick_r | 32 | <u>376</u> | <u>211</u> | 374 | 213 | 379 | 210 | | | | | | | |
| 544.nab_r | 32 | 348 | 155 | <u>348</u> | <u>155</u> | 348 | 155 | | | | | | | |
| 549.fotonik3d_r | 32 | <u>1200</u> | <u>104</u> | 1202 | 104 | 1199 | 104 | | | | | | | |
| 554.roms_r | 32 | 851 | 59.8 | 849 | 59.9 | <u>850</u> | <u>59.8</u> | | | | | | | |

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2019

Hardware Availability: Apr-2019

Software Availability: Nov-2018

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Disabled

IMC Interleaving set to Auto

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

running on linux-jimm Sun Apr 28 02:20:38 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz

2 "physical id"s (chips)

32 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 8

siblings : 16

physical 0: cores 0 1 2 3 4 5 6 7

physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 32

On-line CPU(s) list: 0-31

Thread(s) per core: 2

Core(s) per socket: 8

Socket(s): 2

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 85

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes (Continued)

```

Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bml hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 11264 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 385637 MB
node 0 free: 379465 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387027 MB
node 1 free: 382539 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10

```

```

From /proc/meminfo
MemTotal: 791209844 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Platform Notes (Continued)

From /etc/*release* /etc/*version*

```
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-jimm 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation,
IBPB, IBRS_FW
```

run-level 3 Apr 27 22:01

```
SPEC is set to: /home/cpu2017
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sda4       btrfs    370G   16G  354G   5% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. C220M5.4.0.2.193.1203182037 12/03/2018
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====
C          | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
```

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2019

Hardware Availability: Apr-2019

Software Availability: Nov-2018

Compiler Version Notes (Continued)

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
C++ | 508.namd_r(base) 510.parest_r(base)
=====

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
C++, C | 511.povray_r(base) 526.blender_r(base)
=====

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
C++, C, Fortran | 507.cactuBSSN_r(base)
=====

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
=====

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
=====

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2019

Hardware Availability: Apr-2019

Software Availability: Nov-2018

Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
```

```
507.cactuBSSN_r: -DSPEC_LP64
```

```
508.namd_r: -DSPEC_LP64
```

```
510.parest_r: -DSPEC_LP64
```

```
511.povray_r: -DSPEC_LP64
```

```
519.lbm_r: -DSPEC_LP64
```

```
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
```

```
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
```

```
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
```

```
538.imagick_r: -DSPEC_LP64
```

```
544.nab_r: -DSPEC_LP64
```

```
549.fotonik3d_r: -DSPEC_LP64
```

```
554.roms_r: -DSPEC_LP64
```



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECrate®2017_fp_base = 107

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2019

Hardware Availability: Apr-2019

Software Availability: Nov-2018

Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2019-04-02.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.2019-04-02.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revI.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-04-28 07:50:37-0400.

Report generated on 2020-08-04 20:01:49 by CPU2017 PDF formatter v6255.

Originally published on 2019-05-14.