SPEC® CPU2017 Floating Point Rate Result

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Inspur Corporation

Inspur NS5162M5 (Intel Xeon Bronze 3104)

SPECrate2017_fp_base =   42.6

SPECrate2017_fp_peak =   43.1

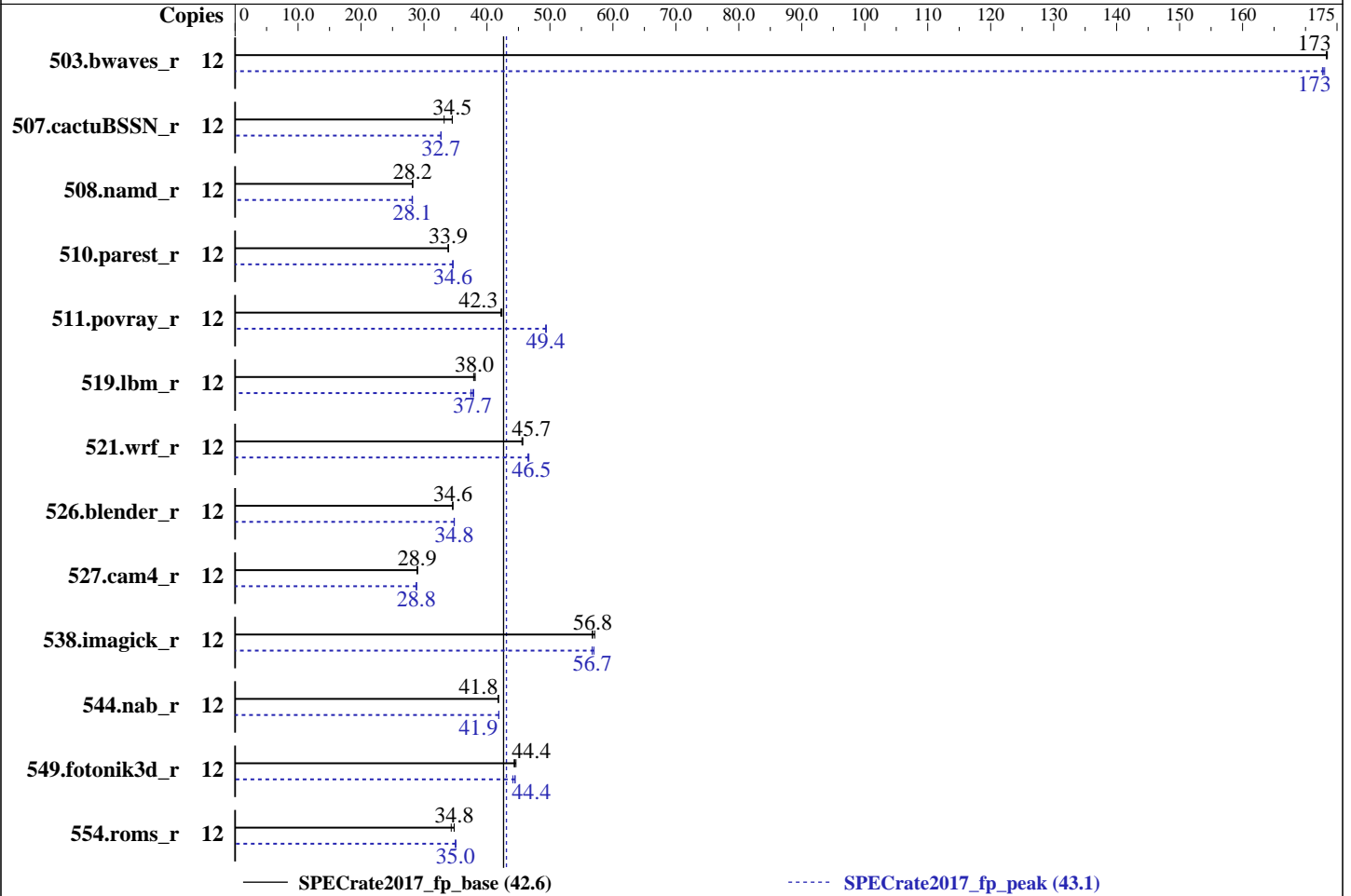**CPU2017 License:** 3358

Test Sponsor: Inspur Corporation

Tested by: Inspur Corporation

Test Date: May-2019

Hardware Availability: Aug-2018

Software Availability: Mar-2018

Benchmark	Copies	Base	Peak
503.bwaves_r	12	173	173
507.cactuBSSN_r	12	34.5	32.7
508.namd_r	12	28.2	28.1
510.parest_r	12	33.9	34.6
511.povray_r	12	42.3	49.4
519.lbm_r	12	38.0	37.7
521.wrf_r	12	45.7	46.5
526.blender_r	12	34.6	34.8
527.cam4_r	12	28.9	28.8
538.imagick_r	12	56.8	56.7
544.nab_r	12	41.8	41.9
549.fotonik3d_r	12	44.4	44.4
554.roms_r	12	34.8	35.0

SPECrate2017_fp_base (42.6)

SPECrate2017_fp_peak (43.1)

Hardware

CPU Name: Intel Xeon Bronze 3104
  Max MHz.:   1700
  Nominal: 1700
Enabled: 12 cores, 2 chips
Orderable: 1,2 chips
Cache L1:   32 KB I + 32 KB D on chip per core
  L2:   1 MB I+D on chip per core
  L3:   8.25 MB I+D on chip per chip
  Other: None
Memory: 192 GB (12 x 16 GB 2Rx4 PC4-2666V-R, running at 2133)
Storage: 1 x 200 GB SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP2
   4.4.120-92.70-default
Compiler: C/C++: Version 18.0.0.128 of Intel C/C++
   Compiler for Linux;
   Fortran: Version 18.0.0.128 of Intel Fortran
   Compiler for Linux
Parallel: No
Firmware: Version 4.0.1 released Aug-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None

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Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	12	694	173	**694**	**173**	694	173	12	695	173	**696**	**173**	697	173
507.cactuBSSN_r	12	**441**	**34.5**	440	34.5	458	33.2	12	**465**	**32.7**	465	32.7	465	32.7
508.namd_r	12	404	28.2	404	28.2	**404**	**28.2**	12	405	**28.1**	405	28.2	405	28.1
510.parest_r	12	928	33.8	926	33.9	**926**	**33.9**	12	907	34.6	909	34.5	**907**	**34.6**
511.povray_r	12	664	42.2	661	42.4	**662**	**42.3**	12	**568**	**49.4**	568	49.3	567	49.4
519.lbm_r	12	**333**	**38.0**	332	38.1	334	37.9	12	334	37.9	338	37.4	**335**	**37.7**
521.wrf_r	12	590	45.6	589	45.7	**589**	**45.7**	12	576	46.7	578	46.5	**578**	**46.5**
526.blender_r	12	**529**	**34.6**	529	34.6	529	34.5	12	525	34.8	526	34.8	**525**	**34.8**
527.cam4_r	12	**725**	**28.9**	724	29.0	726	28.9	12	730	28.8	**729**	**28.8**	728	28.8
538.imagick_r	12	522	57.1	**525**	**56.8**	526	56.7	12	524	57.0	526	56.7	**526**	**56.7**
544.nab_r	12	**483**	**41.8**	483	41.8	483	41.8	12	**482**	**41.9**	482	41.9	482	41.9
549.fotonik3d_r	12	1048	44.6	**1053**	**44.4**	1055	44.3	12	1060	44.1	**1052**	**44.4**	1052	44.5
554.roms_r	12	556	34.3	548	34.8	**548**	**34.8**	12	**545**	**35.0**	545	35.0	544	35.1
SPECrate2017_fp_base =		**42.6**											
SPECrate2017_fp_peak =		**43.1**											

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/CPU2017/lib/ia32:/home/CPU2017/lib/intel64:/home/CPU2017/je5.0.1-32:/home/CPU2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

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General Notes (Continued)

```
     is mitigated in the system as tested and documented.
     Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
     is mitigated in the system as tested and documented.
     Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
     is mitigated in the system as tested and documented.
```

Platform Notes

```
     BIOS and OS configuration:
     SCALING_GOVERNOR set to Performance
     Hardware Prefetch set to Disable
     VT Support set to Disable
     C1E Support set to Disable
     IMC (Integrated memory controller) Interleaving set to 1-way
     Sub NUMA Cluster (SNC) set to Enable
     Sysinfo program /home/CPU2017/bin/sysinfo
     Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
     running on linux-obz8 Sat May 11 03:10:47 2019

     SUT (System Under Test) info as seen by some common utilities.
     For more information on this section, see
        https://www.spec.org/cpu2017/Docs/config.html#sysinfo

     From /proc/cpuinfo
        model name : Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
           2  "physical id"s (chips)
           12 "processors"
        cores, siblings (Caution: counting these is hw and system dependent. The following
        excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
           cpu cores : 6
           siblings  : 6
           physical 0: cores 0 1 2 3 4 5
           physical 1: cores 0 1 2 3 4 5

     From lscpu:
        Architecture:          x86_64
        CPU op-mode(s):        32-bit, 64-bit
        Byte Order:            Little Endian
        CPU(s):                12
        On-line CPU(s) list:   0-11
        Thread(s) per core:    1
        Core(s) per socket:    6
        Socket(s):             2
        NUMA node(s):          2
        Vendor ID:             GenuineIntel
```

(Continued on next page)

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Platform Notes (Continued)

```
          CPU family:            6
          Model:                 85
          Model name:            Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
          Stepping:              4
          CPU MHz:               1700.000
          CPU max MHz:           1700.0000
          CPU min MHz:           800.0000
          BogoMIPS:              3392.03
          Virtualization:        VT-x
          L1d cache:             32K
          L1i cache:             32K
          L2 cache:              1024K
          L3 cache:              8448K
          NUMA node0 CPU(s):     0-5
          NUMA node1 CPU(s):     6-11
          Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch arat epb invpcid_single pln pts dtherm hwp
    hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp retpoline
    kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep
    bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt clwb
    avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

 /proc/cpuinfo cache data
    cache size : 8448 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5
    node 0 size: 96208 MB
    node 0 free: 89628 MB
    node 1 cpus: 6 7 8 9 10 11
    node 1 size: 96627 MB
    node 1 free: 91719 MB
    node distances:
    node   0   1
      0:  10  21
      1:  21  10

 From /proc/meminfo
    MemTotal:       197464420 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB
```

(Continued on next page)

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Platform Notes (Continued)

```
/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 2
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-obz8 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
   x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 10 17:58 last=5

SPEC is set to: /home/CPU2017
   Filesystem      Type  Size  Used Avail Use% Mounted on
   /dev/sda4       xfs   145G   84G   61G  59% /home

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Inspur 4.0.1 08/30/2018
   Memory:
    12x Micron 18ASF2G72PZ-2G6D1 16 GB 1 rank 2666, configured at 2133
    4x NO DIMM NO DIMM

(End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
CC  519.lbm_r(base) 538.imagick_r(base, peak) 544.nab_r(base)
------------------------------------------------------------------------------
```

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Compiler Version Notes (Continued)

```
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
CC   519.lbm_r(peak) 544.nab_r(peak)
------------------------------------------------------------------------------
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CXXC 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
CXXC 508.namd_r(peak) 510.parest_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CC   511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
CC   511.povray_r(peak) 526.blender_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC  507.cactuBSSN_r(base)
------------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
```

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Compiler Version Notes (Continued)

```
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
FC   507.cactuBSSN_r(peak)
------------------------------------------------------------------------
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
 FC  503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base)
------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
FC   554.roms_r(peak)
------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
 CC  521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------


==============================================================================
CC   521.wrf_r(peak) 527.cam4_r(peak)
------------------------------------------------------------------------
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
icc (ICC) 18.0.0 20170811
```

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Compiler Version Notes (Continued)

```
Copyright (C) 1985-2017 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
```
icc
```

C++ benchmarks:
```
icpc
```

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using both C and C++:
```
icpc icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

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Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Base Other Flags

C benchmarks:

```
-m64 -std=c11
```

C++ benchmarks:

```
-m64
```

Fortran benchmarks:

```
-m64
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11
```

Benchmarks using both C and C++:

```
-m64 -std=c11
```

(Continued on next page)

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Base Other Flags (Continued)

Benchmarks using Fortran, C, and C++:
```
-m64 -std=c11
```

Peak Compiler Invocation

C benchmarks:
```
icc
```

C++ benchmarks:
```
icpc
```

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using both C and C++:
```
icpc icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

519.lbm_r: `-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

538.imagick_r: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3`

544.nab_r: `Same as 519.lbm_r`

(Continued on next page)

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Peak Optimization Flags (Continued)

C++ benchmarks:
```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Fortran benchmarks:

```
 503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3
-nostandard-realloc-lhs -align array32byte
```

```
 549.fotonik3d_r: Same as 503.bwaves_r
```

```
 554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:
```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:
```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3
```

Benchmarks using Fortran, C, and C++:
```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
```

Peak Other Flags

C benchmarks:
```
-m64 -std=c11
```

C++ benchmarks:
```
-m64
```

Fortran benchmarks:
```
-m64
```

(Continued on next page)

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Inspur Corporation

Inspur NS5162M5 (Intel Xeon Bronze 3104)

SPECrate2017_fp_base =   42.6

SPECrate2017_fp_peak =   43.1

CPU2017 License: 3358
Test Sponsor: Inspur Corporation
Tested by: Inspur Corporation

Test Date: May-2019
Hardware Availability: Aug-2018
Software Availability: Mar-2018

Peak Other Flags (Continued)

Benchmarks using both Fortran and C:
```
-m64 -std=c11
```

Benchmarks using both C and C++:
```
-m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```
-m64 -std=c11
```

The flags files that were used to format this result can be browsed at
```
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.1-SKL.html
```

You can also download the XML flags sources by saving the following links:
```
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Inspur-Platform-Settings-V1.1-SKL.xml
```

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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