



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

CPU2017 License: 9019

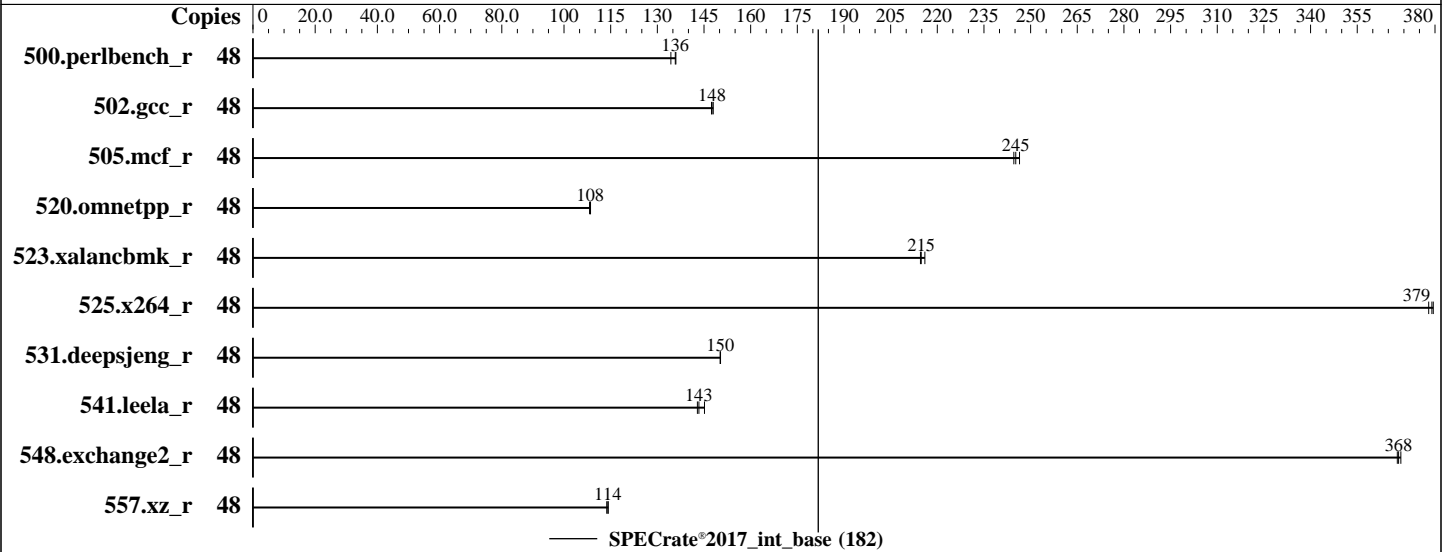
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 6246  
 Max MHz: 4200  
 Nominal: 3300  
 Enabled: 24 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 24.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Desktop 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4g released Jul-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: None  
 Power Management: --



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Aug-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	48	569	134	<b>563</b>	<b>136</b>	562	136							
502.gcc_r	48	461	147	459	148	<b>460</b>	<b>148</b>							
505.mcf_r	48	315	246	317	245	<b>316</b>	<b>245</b>							
520.omnetpp_r	48	<b>581</b>	<b>108</b>	580	109	582	108							
523.xalancbmk_r	48	235	216	<b>236</b>	<b>215</b>	236	215							
525.x264_r	48	<b>222</b>	<b>379</b>	222	378	222	379							
531.deepsjeng_r	48	<b>366</b>	<b>150</b>	366	150	366	150							
541.leela_r	48	548	145	<b>554</b>	<b>143</b>	556	143							
548.exchange2_r	48	<b>341</b>	<b>368</b>	342	368	341	369							
557.xz_r	48	456	114	<b>454</b>	<b>114</b>	454	114							

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes

#### BIOS Settings:

Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on linux-56kd Wed Aug 7 12:46:31 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

#### From /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
 2 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 12
siblings       : 24
physical 0:    cores 0 2 4 8 10 17 18 19 20 24 25 27
physical 1:    cores 0 2 8 9 10 17 18 19 20 25 26 27
```

#### From lscpu:

```
Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s):       2
NUMA node(s):   4
Vendor ID:       GenuineIntel
CPU family:      6
Model:           85
Model name:      Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
Stepping:        7
CPU MHz:         3300.000
CPU max MHz:     4200.0000
CPU min MHz:     1200.0000
BogoMIPS:        6600.00
Virtualization:  VT-x
L1d cache:      32K
L1i cache:      32K
L2 cache:       1024K
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

### Platform Notes (Continued)

```

L3 cache:                25344K
NUMA node0 CPU(s):      0,1,3,5,9,10,24,25,27,29,33,34
NUMA node1 CPU(s):      2,4,6-8,11,26,28,30-32,35
NUMA node2 CPU(s):      12-15,17,21,36-39,41,45
NUMA node3 CPU(s):      16,18-20,22,23,40,42-44,46,47
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 25344 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0 1 3 5 9 10 24 25 27 29 33 34
node 0 size: 192063 MB
node 0 free: 191748 MB
node 1 cpus: 2 4 6 7 8 11 26 28 30 31 32 35
node 1 size: 193523 MB
node 1 free: 193259 MB
node 2 cpus: 12 13 14 15 17 21 36 37 38 39 41 45
node 2 size: 193523 MB
node 2 free: 193282 MB
node 3 cpus: 16 18 19 20 22 23 40 42 43 44 46 47
node 3 size: 193520 MB
node 3 free: 193262 MB
node distances:
node  0  1  2  3
 0:  10  11  21  21
 1:  11  10  21  21
 2:  21  21  10  11
 3:  21  21  11  10

```

```

From /proc/meminfo
MemTotal:       791173828 kB
HugePages_Total:       0
Hugepagesize:     2048 kB

```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

From /etc/*release* /etc/*version*
os-release:
  NAME="SLED"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
  ID="sled"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sled:15"

uname -a:
  Linux linux-56kd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown):          Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation,
IBPB, IBRS_FW

run-level 3 Aug 7 12:44

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda1       xfs   894G   22G  872G   3% /

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4g.0.0712190011 07/12/2019
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

```

### Compiler Version Notes

```

=====
C      | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
      | 525.x264_r(base) 557.xz_r(base)
=====

```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====  
C++ | 520.omnetpp\_r(base) 523.xalancbmk\_r(base) 531.deepsjeng\_r(base)  
| 541.leela\_r(base)  
=====

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 548.exchange2\_r(base)  
=====

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

500.perlbenc\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64  
502.gcc\_r: -DSPEC\_LP64  
505.mcf\_r: -DSPEC\_LP64  
520.omnetpp\_r: -DSPEC\_LP64  
523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX  
525.x264\_r: -DSPEC\_LP64  
531.deepsjeng\_r: -DSPEC\_LP64  
541.leela\_r: -DSPEC\_LP64  
548.exchange2\_r: -DSPEC\_LP64

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECrate®2017\_int\_base = 182

SPECrate®2017\_int\_peak = Not Run

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Base Portability Flags (Continued)

557.xz\_r: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-07 03:16:31-0400.

Report generated on 2020-07-01 22:20:23 by CPU2017 PDF formatter v6255.

Originally published on 2019-09-06.