



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Threads

600.perlbench_s

602.gcc_s

605.mcf_s

620.omnetpp_s

623.xalanbmk_s

625.x264_s

631.deepsjeng_s

641.leela_s

648.exchange2_s

657.xz_s

Hardware

CPU Name: Intel Xeon Platinum 8253
Max MHz: 3000
Nominal: 2200
Enabled: 32 cores / 32 chips
Orderable: 1, 32 chips
Cache L1: 32 KB I + 32 KB D on chip per core
Cache L2: 1 MB I+D on chip per core
Cache L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: --



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Results Table

Benchmark	Base						Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
602.gcc_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
605.mcf_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
620.omnetpp_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
623.xalancbmk_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
625.x264_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
631.deepsjeng_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
641.leela_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
648.exchange2_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
657.xz_s	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binary compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

sync; echo 3> /proc/sys/vm/drop_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Disabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Disabled

IMC Interleaving set to Auto

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

running on linux-pp10 Wed Aug 28 16:08:04 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz

2 "physical id"s (chips)

2 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 16

siblings : 16

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:

Architecture: x86_64

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```

CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s):           2
NUMA node(s):       2
Vendor ID:           GenuineIntel
CPU family:          63
Model:               85
Model name:          Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
Stepping:            0
CPU MHz:             2200.000
CPU max MHz:         3000.0000
CPU min MHz:         2000.0000
BogoMIPS:            4400.00
Virtualization:     VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sbno fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

```
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
```

```
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385429 MB
node 0 free: 384841 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387045 MB
node 1 free: 386662 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10
```

```
From /proc/meminfo
MemTotal: 790014168 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 28 16:01

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdc2	btrfs	22G	52G	169G	24%	/home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

Memory:

2 x 0xC00 M3934K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

```

=====
C | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
  | 625.x264_s(base) 657.xz_s(base)
=====

```

```

-----
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----

```

```

=====
C++ | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
    | 641.leela_s(base)
=====

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
Fortran | 648.exchange2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fort benchmarks:

ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64

602.gcc_s: -DSPEC_LP64

605.mcf_s: -DSPEC_LP64

620.omnetpp_s: -DSPEC_LP64

623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX

625.x264_s: -DSPEC_LP64

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Base Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -openmp -DSPEC_OPENMP
-L/usr/local/jc5.0.1_64/lib -ljemalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/Intel/compilers_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-lqkmalloc -lrealloc-lhs

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECspeed®2017_int_base =

SPECspeed®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Non-Compliant

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-28 19:08:04-0400.
Report generated on 2020-12-15 19:44:57 by CPU2017 PDF formatter v6255.
Originally published on 2019-09-19.