



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Copies

- 500.perlbench_r
- 502.gcc_r
- 505.mcf_r
- 520.omnetpp_r
- 523.xalanbmk_r
- 525.x264_r
- 531.deepsjeng_r
- 541.leela_r
- 548.exchange2_r
- 557.xz_r

Hardware

CPU Name: Intel Xeon Platinum 8253
 Max MHz: 3000
 Nominal: 2200
 Enabled: 32 cores / 2 chips, 2 threads/core
 Orderable: 1, 2 chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 Cache L2: 1 MB I+D on chip per core
 Cache L3: 22 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
 Storage: 1 x 240 GB M.2 SATA SSD
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.4b released Apr-2019
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: None
 Power Management: --



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Results Table

Benchmark	Base						Peak							
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
502.gcc_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
505.mcf_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
520.omnetpp_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
523.xalancbmk_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
525.x264_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
531.deepsjeng_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
541.leela_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
548.exchange2_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
557.xz_r	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

(Continued on next page)



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)

Prior to runcpu invocation

Filesystem page cache synced and cleared with

sync; echo 3> /proc/sys/vm/drop_caches

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

CPU performance set to Enterprise

Power Performance Tuning set to OS Controls

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

System program /home/cpu2017/bin/sysinfo

Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9

running on linux-db10 Mon Aug 26 12:09:28 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz

2 "physical id"s (chips)

64 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 16

siblings : 32

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Continued on next page)



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:

```

Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 64
On-line CPU(s) list:   0-63
Thread(s) per core:    2
Core(s) per socket:    2
Socket(s):              2
NUMA node(s):          4
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
Stepping:               6
CPU MHz:                2200.000
CPU max MHz:            3000.0000
CPU min MHz:            1000.0000
BogoMIPS:               4400.00
Virtualization:        VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               22528K
NUMA node0 CPU(s):     0-3,8-11,32-35,40-43
NUMA node1 CPU(s):     4-7,12-15,36-39,44-47
NUMA node2 CPU(s):     16-19,24-27,48-51,56-59
NUMA node3 CPU(s):     20-23,28-31,52-55,60-63
Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept

```

(Continued on next page)



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```
vpid fsgsbase tsc_adjust bml hle avx512f smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ies ssod
```

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 8 9 10 11 32 33 34 35 40 41 42 43
node 0 size: 191882 MB
node 0 free: 191178 MB
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47
node 1 size: 193222 MB
node 1 free: 19328 MB
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59
node 2 size: 193222 MB
node 2 free: 193289 MB
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
node 3 size: 193519 MB
node 3 free: 193287 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10
```

```
From /proc/meminfo
MemTotal: 791007684 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*
```

(Continued on next page)



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Platform Notes (Continued)

```

os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

```

```

uname -a:
Linux linux-dbl0 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

```

CVE-2017-5754 (Meltdown) Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation,
IBPB, IBRS_FW

```

run-level 3 1 23 10:15

```

df -h to: /home/cpu2017
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sda2       btrfs    222G   52G  170G  24% /home

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

Memory:

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes

```
=====  
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)  
          | 525.x264_r(base) 557.xz_r(base)  
=====
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

```
=====  
C++       | 520.omnetpp_r(base) 521.balancebm_r(base) 531.deepsjeng_r(base)  
          | 541.leela_r(base)  
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

```
=====  
Fortran   | 508.exchange2_r(base)  
=====
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
=====
```

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64



SPEC CPU®2017 Integer Rate Results

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG

Guidelines for General Availability and the SPEC CPU 2017 run and reporting

rules. Specifically, the submitter has notified SPEC that the system was run

with a CPU that is not supported by Cisco with the given system configuration.

Base Portability Flags

```

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

```

Base Optimization Flags

C benchmarks:

```

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

```

C++ benchmarks:

```

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

```

Fortran benchmarks:

```

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

```




SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrate®2017_int_base =

SPECrate®2017_int_peak =

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-Platinum-8253-19.0ul-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML files sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-Platinum-8253-19.0ul-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

Non-Compliant

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-08-26 15:09:28-0400.

Report generated on 2020-12-15 19:44:58 by CPU2017 PDF formatter v6255.

Originally published on 2019-09-19.