



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

SPECrate®2017\_fp\_base = 506

SPECrate®2017\_fp\_peak = 513

CPU2017 License: 9019

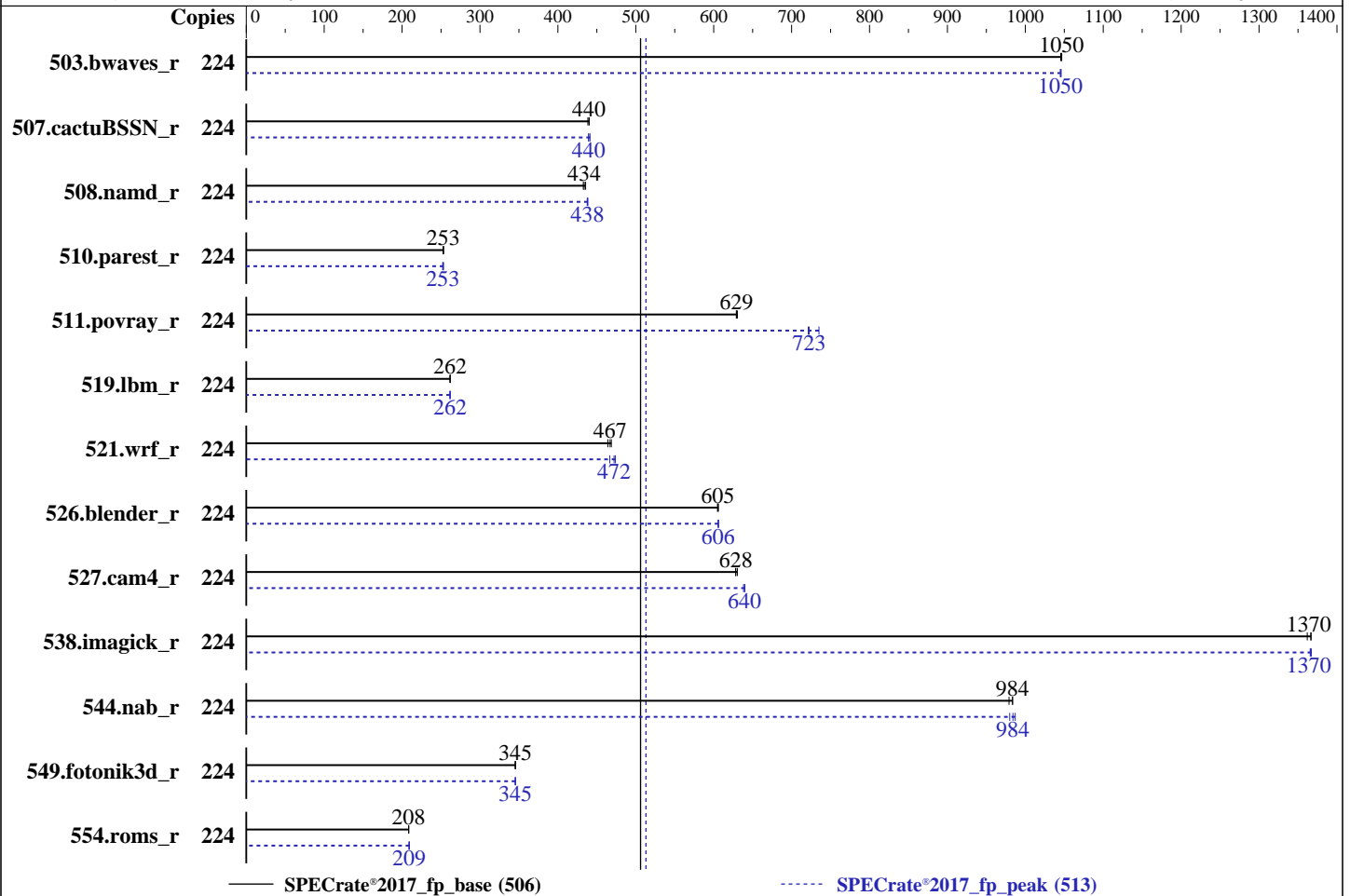
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Oct-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Platinum 8276  
 Max MHz: 4000  
 Nominal: 2200  
 Enabled: 112 cores, 4 chips, 2 threads/core  
 Orderable: 2,4 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 38.5 MB I+D on chip per chip  
 Other: None  
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 1.9 TB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Desktop 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4b released Apr-2019  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: default



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	224	2146	1050	<u>2146</u>	<u>1050</u>	2149	1050	224	2149	1050	2147	1050	<u>2149</u>	<u>1050</u>
507.cactuBSSN_r	224	644	440	647	438	<u>645</u>	<u>440</u>	224	645	439	643	441	<u>645</u>	<u>440</u>
508.namd_r	224	492	433	<u>491</u>	<u>434</u>	489	436	224	485	438	486	438	<u>486</u>	<u>438</u>
510.parest_r	224	2315	253	2318	253	<u>2316</u>	<u>253</u>	224	2324	252	2315	253	<u>2319</u>	<u>253</u>
511.povray_r	224	830	630	832	629	<u>831</u>	<u>629</u>	224	725	721	712	735	<u>724</u>	<u>723</u>
519.lbm_r	224	902	262	902	262	<u>902</u>	<u>262</u>	224	<u>902</u>	<u>262</u>	903	262	902	262
521.wrf_r	224	1081	464	<u>1075</u>	<u>467</u>	1071	469	224	1059	474	1075	467	<u>1063</u>	<u>472</u>
526.blender_r	224	<u>564</u>	<u>605</u>	564	605	563	606	224	<u>563</u>	<u>606</u>	563	606	563	606
527.cam4_r	224	<u>623</u>	<u>628</u>	622	630	624	628	224	612	640	614	638	<u>613</u>	<u>640</u>
538.imagick_r	224	<u>408</u>	<u>1370</u>	409	1360	408	1370	224	407	1370	408	1370	<u>408</u>	<u>1370</u>
544.nab_r	224	383	984	385	979	<u>383</u>	<u>984</u>	224	385	980	<u>383</u>	<u>984</u>	382	987
549.fotonik3d_r	224	2528	345	2527	345	<u>2528</u>	<u>345</u>	224	<u>2527</u>	<u>345</u>	2527	345	2528	345
554.roms_r	224	<u>1708</u>	<u>208</u>	1708	208	1706	209	224	1700	209	<u>1703</u>	<u>209</u>	1703	209

SPECrate®2017\_fp\_base = **506**

SPECrate®2017\_fp\_peak = **513**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches

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### General Notes (Continued)

runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
running on linux-0enh Fri Oct 18 09:02:42 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Platinum 8276 CPU @ 2.20GHz  
4 "physical id"s (chips)  
224 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 28  
siblings : 56  
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30  
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30  
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30  
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian

(Continued on next page)



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### Platform Notes (Continued)

```

CPU(s):                224
On-line CPU(s) list:  0-223
Thread(s) per core:   2
Core(s) per socket:   28
Socket(s):            4
NUMA node(s):        8
Vendor ID:            GenuineIntel
CPU family:           6
Model:                85
Model name:           Intel(R) Xeon(R) Platinum 8276 CPU @ 2.20GHz
Stepping:             7
CPU MHz:              2200.000
CPU max MHz:          4000.0000
CPU min MHz:          1000.0000
BogoMIPS:             4400.00
Virtualization:       VT-x
L1d cache:            32K
L1i cache:            32K
L2 cache:             1024K
L3 cache:             39424K
NUMA node0 CPU(s):   0-3,7-9,14-17,21-23,112-115,119-121,126-129,133-135
NUMA node1 CPU(s):   4-6,10-13,18-20,24-27,116-118,122-125,130-132,136-139
NUMA node2 CPU(s):   28-31,35-37,42-45,49-51,140-143,147-149,154-157,161-163
NUMA node3 CPU(s):   32-34,38-41,46-48,52-55,144-146,150-153,158-160,164-167
NUMA node4 CPU(s):   56-59,63-65,70-73,77-79,168-171,175-177,182-185,189-191
NUMA node5 CPU(s):   60-62,66-69,74-76,80-83,172-174,178-181,186-188,192-195
NUMA node6 CPU(s):   84-87,91-93,98-101,105-107,196-199,203-205,210-213,217-219
NUMA node7 CPU(s):   88-90,94-97,102-104,108-111,200-202,206-209,214-216,220-223
Flags:                fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpelt rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```
/proc/cpuinfo cache data
cache size : 39424 KB
```

```
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 8 nodes (0-7)
```

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### Platform Notes (Continued)

```

node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 112 113 114 115 119 120 121 126 127 128
129 133 134 135
node 0 size: 191934 MB
node 0 free: 177363 MB
node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 116 117 118 122 123 124 125 130 131
132 136 137 138 139
node 1 size: 193525 MB
node 1 free: 182465 MB
node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 140 141 142 143 147 148 149 154
155 156 157 161 162 163
node 2 size: 193525 MB
node 2 free: 182483 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 144 145 146 150 151 152 153 158
159 160 164 165 166 167
node 3 size: 193525 MB
node 3 free: 182497 MB
node 4 cpus: 56 57 58 59 63 64 65 70 71 72 73 77 78 79 168 169 170 171 175 176 177 182
183 184 185 189 190 191
node 4 size: 193525 MB
node 4 free: 182434 MB
node 5 cpus: 60 61 62 66 67 68 69 74 75 76 80 81 82 83 172 173 174 178 179 180 181 186
187 188 192 193 194 195
node 5 size: 193525 MB
node 5 free: 182491 MB
node 6 cpus: 84 85 86 87 91 92 93 98 99 100 101 105 106 107 196 197 198 199 203 204 205
210 211 212 213 217 218 219
node 6 size: 193525 MB
node 6 free: 182491 MB
node 7 cpus: 88 89 90 94 95 96 97 102 103 104 108 109 110 111 200 201 202 206 207 208
209 214 215 216 220 221 222 223
node 7 size: 193493 MB
node 7 free: 182464 MB
node distances:
node  0  1  2  3  4  5  6  7
0:  10 11 21 21 21 21 21 21
1:  11 10 21 21 21 21 21 21
2:  21 21 10 11 21 21 21 21
3:  21 21 11 10 21 21 21 21
4:  21 21 21 21 10 11 21 21
5:  21 21 21 21 11 10 21 21
6:  21 21 21 21 21 21 10 11
7:  21 21 21 21 21 21 11 10

```

From /proc/meminfo

MemTotal: 1583698936 kB

HugePages\_Total: 0

Hugepagesize: 2048 kB

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### Platform Notes (Continued)

From /etc/\*release\* /etc/\*version\*

```
os-release:
  NAME="SLED"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
  ID="sled"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sled:15"
```

```
uname -a:
Linux linux-0enh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault):          No status reported
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
Speculation, IBPB, IBRS_FW
```

run-level 3 Oct 17 23:04

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal       xfs   224G  110G  115G  49% /
```

```
From /sys/devices/virtual/dmi/id
BIOS:      Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
Vendor:    Cisco Systems Inc
Product:   UCSB-B480-M5
Serial:    FLM2230020U
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:  
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)



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### Compiler Version Notes

```
=====
C | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
  | 544.nab_r(base, peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C | 511.povray_r(base, peak) 526.blender_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
         | 554.roms_r(base, peak)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```

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### Compiler Version Notes (Continued)

64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----  
=====  
Fortran, C | 521.wrf\_r(base, peak) 527.cam4\_r(base, peak)  
-----

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

### Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

### Base Portability Flags

503.bwaves\_r: -DSPEC\_LP64  
507.cactuBSSN\_r: -DSPEC\_LP64  
508.namd\_r: -DSPEC\_LP64  
510.parest\_r: -DSPEC\_LP64  
511.povray\_r: -DSPEC\_LP64  
519.lbm\_r: -DSPEC\_LP64

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## Base Portability Flags (Continued)

```
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

(Continued on next page)



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## Peak Compiler Invocation (Continued)

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4
```

```
538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4
```

544.nab\_r: Same as 538.imagick\_r

C++ benchmarks:

```
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4
```

```
510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

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## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Platinum 8276, 2.20GHz)

SPECrate®2017\_fp\_base = 506

SPECrate®2017\_fp\_peak = 513

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Oct-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

Fortran benchmarks:

```
503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

549.fotonik3d\_r: Same as 503.bwaves\_r

```
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both Fortran and C:

```
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
```

```
526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>  
<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>



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