



SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECrate®2017_int_base = 421

SPECrate®2017_int_peak = 439

CPU2017 License: 9019

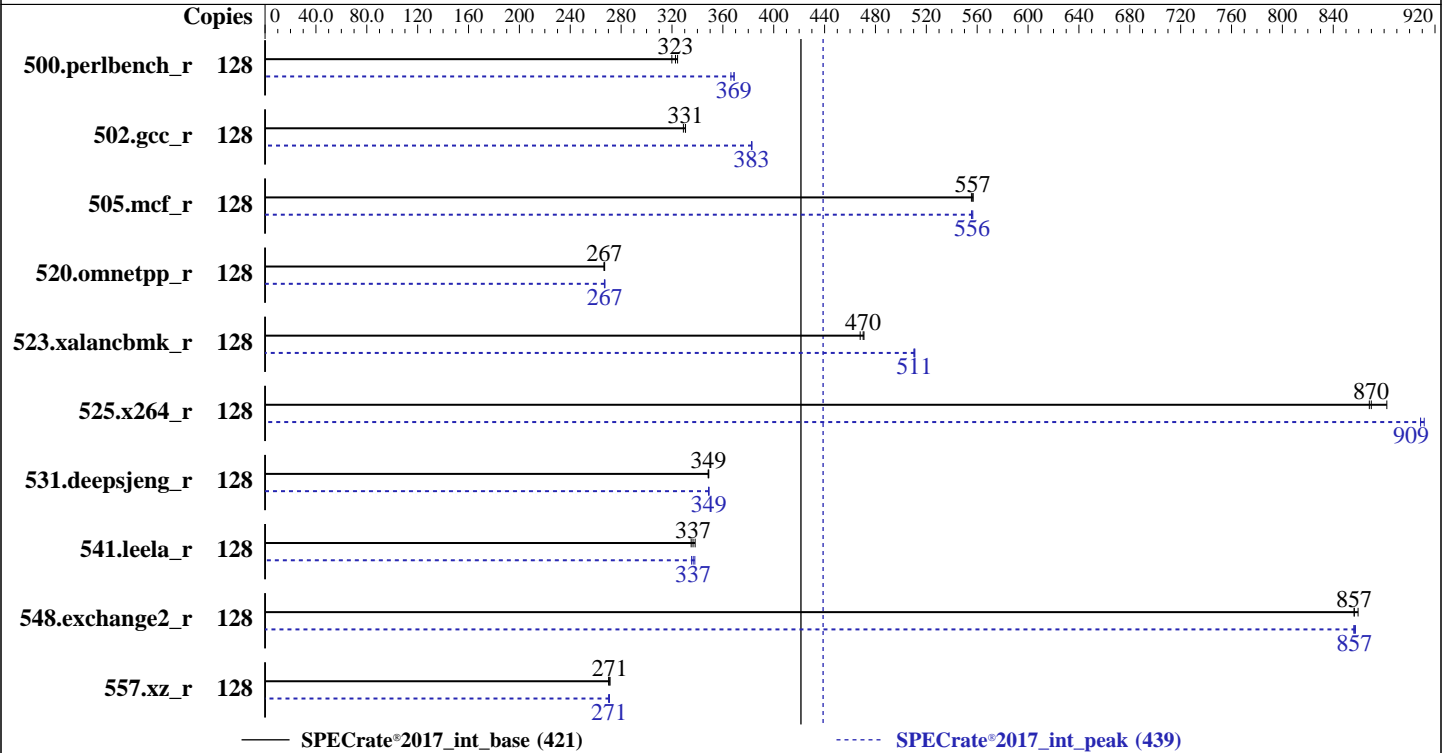
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Dec-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



Hardware

CPU Name: Intel Xeon Gold 6242
 Max MHz: 3900
 Nominal: 2800
 Enabled: 64 cores, 4 chips, 2 threads/core
 Orderable: 2,4 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 22 MB I+D on chip per chip
 Other: None
 Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
 Storage: 1 x 1.9 TB SSD SAS
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
 Parallel: No
 Firmware: Version 4.0.4b released Apr-2019
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 32/64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer performance at the cost of additional power usage



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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	128	631	323	637	320	628	324	128	552	369	556	366	553	369
502.gcc_r	128	551	329	548	331	548	331	128	474	383	473	383	474	383
505.mcf_r	128	372	557	371	557	372	555	128	372	556	372	556	372	557
520.omnetpp_r	128	630	266	629	267	629	267	128	629	267	629	267	629	267
523.xalancbmk_r	128	289	468	287	471	287	470	128	265	511	265	510	265	511
525.x264_r	128	258	868	258	870	254	882	128	247	909	246	912	247	909
531.deepsjeng_r	128	421	348	421	349	420	349	128	421	349	420	349	420	349
541.leela_r	128	627	338	630	337	633	335	128	630	337	627	338	632	335
548.exchange2_r	128	392	857	392	856	390	859	128	391	857	392	856	391	857
557.xz_r	128	512	270	510	271	510	271	128	510	271	511	271	512	270

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

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General Notes (Continued)

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled

SNC set to Enabled

IMC Interleaving set to 1-way Interleave

Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011

running on linux-icbf Thu Dec 12 21:14:49 2019

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
```

```
4 "physical id"s (chips)
```

```
128 "processors"
```

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 16
```

```
siblings : 32
```

```
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

```
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

```
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

```
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 128

On-line CPU(s) list: 0-127

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Platform Notes (Continued)

```

Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 8
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
Stepping: 6
CPU MHz: 2800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 5600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-3,8-11,64-67,72-75
NUMA node1 CPU(s): 4-7,12-15,68-71,76-79
NUMA node2 CPU(s): 16-19,24-27,80-83,88-91
NUMA node3 CPU(s): 20-23,28-31,84-87,92-95
NUMA node4 CPU(s): 32-35,40-43,96-99,104-107
NUMA node5 CPU(s): 36-39,44-47,100-103,108-111
NUMA node6 CPU(s): 48-51,56-59,112-115,120-123
NUMA node7 CPU(s): 52-55,60-63,116-119,124-127
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdp1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

```
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 8 nodes (0-7)
node 0 cpus: 0 1 2 3 8 9 10 11 64 65 66 67 72 73 74 75
node 0 size: 192096 MB
```

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Platform Notes (Continued)

```

node 0 free: 191860 MB
node 1 cpus: 4 5 6 7 12 13 14 15 68 69 70 71 76 77 78 79
node 1 size: 193527 MB
node 1 free: 193369 MB
node 2 cpus: 16 17 18 19 24 25 26 27 80 81 82 83 88 89 90 91
node 2 size: 193527 MB
node 2 free: 193389 MB
node 3 cpus: 20 21 22 23 28 29 30 31 84 85 86 87 92 93 94 95
node 3 size: 193527 MB
node 3 free: 193381 MB
node 4 cpus: 32 33 34 35 40 41 42 43 96 97 98 99 104 105 106 107
node 4 size: 193527 MB
node 4 free: 193378 MB
node 5 cpus: 36 37 38 39 44 45 46 47 100 101 102 103 108 109 110 111
node 5 size: 193527 MB
node 5 free: 193356 MB
node 6 cpus: 48 49 50 51 56 57 58 59 112 113 114 115 120 121 122 123
node 6 size: 193527 MB
node 6 free: 193392 MB
node 7 cpus: 52 53 54 55 60 61 62 63 116 117 118 119 124 125 126 127
node 7 size: 193496 MB
node 7 free: 193359 MB
node distances:
node   0   1   2   3   4   5   6   7
  0:  10  11  21  21  21  21  21  21
  1:  11  10  21  21  21  21  21  21
  2:  21  21  10  11  21  21  21  21
  3:  21  21  11  10  21  21  21  21
  4:  21  21  21  21  10  11  21  21
  5:  21  21  21  21  11  10  21  21
  6:  21  21  21  21  21  21  10  11
  7:  21  21  21  21  21  21  11  10

```

From /proc/meminfo

```

MemTotal:      1583880732 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/*release* /etc/*version*

```

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"

```

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Platform Notes (Continued)

CPE_NAME="cpe:/o:suse:sles:15"

uname -a:

```
Linux linux-icbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):	No status reported
Microarchitectural Data Sampling:	No status reported
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Dec 12 21:06

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdb2	btrfs	222G	8.5G	213G	4%	/home

From /sys/devices/virtual/dmi/id

```
BIOS: Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
Vendor: Cisco Systems Inc
Product: UCSB-B480-M5
Serial: FLM230102QU
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

=====
C | 502.gcc_r(peak)

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

```
=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 502.gcc_r(peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C          | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 523.xalanbmk_r(peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 520.omnetpp_r(base, peak) 523.xalanbmk_r(base)
          | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 523.xalanbmk_r(peak)
-----
```

(Continued on next page)



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Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

=====
Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64

502.gcc_r: -DSPEC_LP64

505.mcf_r: -DSPEC_LP64

520.omnetpp_r: -DSPEC_LP64

523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX

525.x264_r: -DSPEC_LP64

531.deepsjeng_r: -DSPEC_LP64

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Base Portability Flags (Continued)

541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502.gcc_r:icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r:icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:

```
ifort -m64
```



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Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r
```

C++ benchmarks:

```
520.omnetpp_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

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Peak Optimization Flags (Continued)

```
523.xalancbmk_r: -w1, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

```
-w1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

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