



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

CPU2017 License: 9019

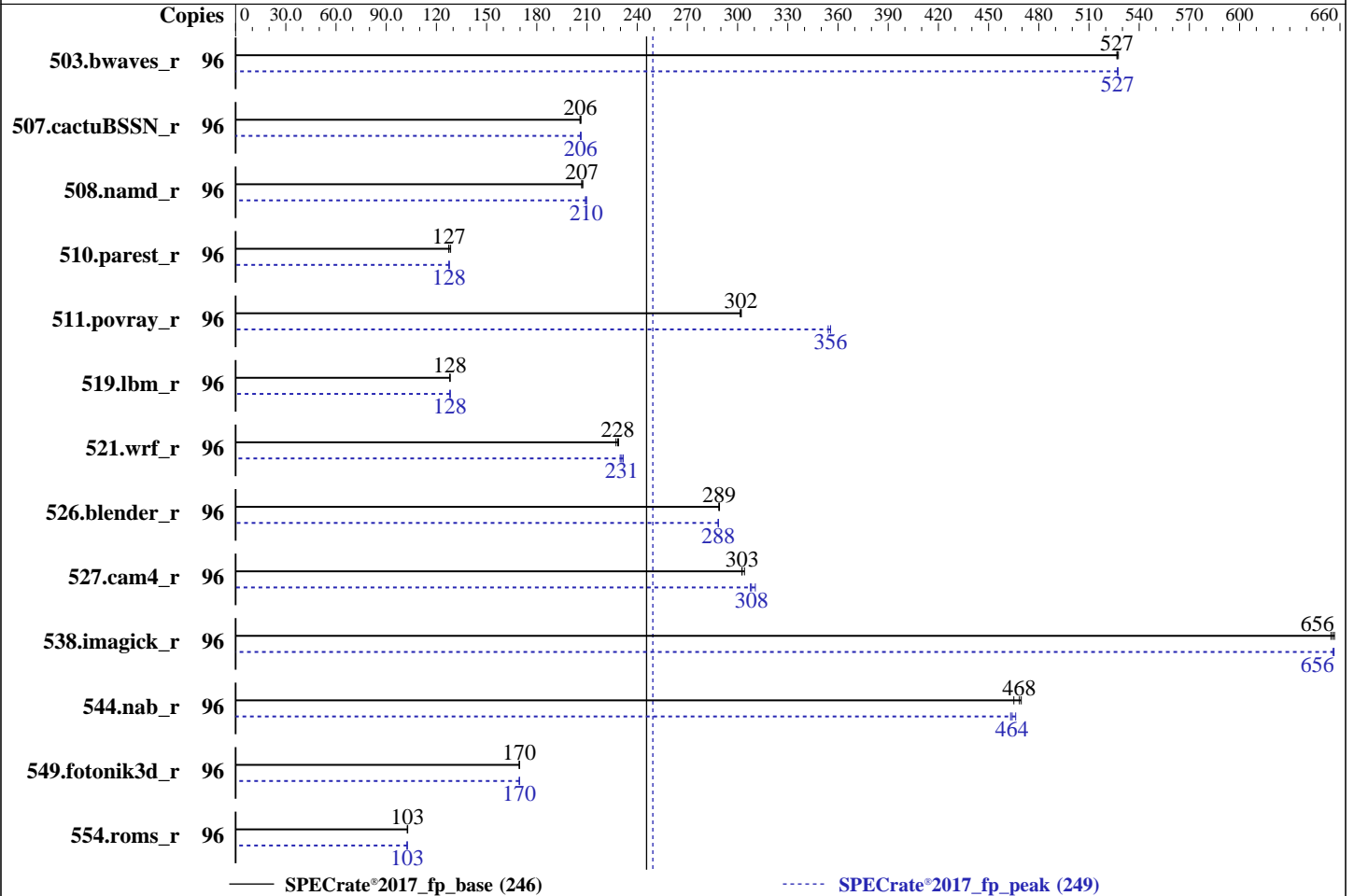
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2020

Hardware Availability: Feb-2020

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Gold 6240R  
 Max MHz: 4000  
 Nominal: 2400  
 Enabled: 48 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 35.75 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
 Storage: 1 x 960 GB SSD SAS  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
 Parallel: No  
 Firmware: Version 4.0.4i released Aug-2019  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: None  
 Power Management: BIOS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Feb-2020

Hardware Availability: Feb-2020

Software Availability: May-2019

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	96	1825	528	1828	527	<b>1828</b>	<b>527</b>	96	1826	527	<b>1826</b>	<b>527</b>	1826	527
507.cactuBSSN_r	96	<b>590</b>	<b>206</b>	590	206	589	206	96	589	206	<b>589</b>	<b>206</b>	590	206
508.namd_r	96	439	208	441	207	<b>441</b>	<b>207</b>	96	435	210	436	209	<b>435</b>	<b>210</b>
510.parest_r	96	<b>1970</b>	<b>127</b>	1971	127	1954	128	96	<b>1969</b>	<b>128</b>	1966	128	1970	128
511.povray_r	96	742	302	743	302	<b>742</b>	<b>302</b>	96	633	354	<b>630</b>	<b>356</b>	630	356
519.lbm_r	96	<b>790</b>	<b>128</b>	790	128	790	128	96	<b>789</b>	<b>128</b>	790	128	789	128
521.wrf_r	96	946	227	<b>942</b>	<b>228</b>	940	229	96	928	232	936	230	<b>932</b>	<b>231</b>
526.blender_r	96	506	289	<b>506</b>	<b>289</b>	506	289	96	507	288	507	289	<b>507</b>	<b>288</b>
527.cam4_r	96	<b>555</b>	<b>303</b>	555	303	552	304	96	546	308	<b>545</b>	<b>308</b>	541	311
538.imagick_r	96	365	655	364	657	<b>364</b>	<b>656</b>	96	364	656	364	656	<b>364</b>	<b>656</b>
544.nab_r	96	347	465	<b>345</b>	<b>468</b>	344	470	96	<b>348</b>	<b>464</b>	349	463	347	466
549.fotonik3d_r	96	2206	170	<b>2206</b>	<b>170</b>	2206	170	96	2205	170	<b>2206</b>	<b>170</b>	2206	170
554.roms_r	96	<b>1486</b>	<b>103</b>	1487	103	1483	103	96	<b>1488</b>	<b>103</b>	1489	102	1487	103

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

### General Notes (Continued)

runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
running on linux-41f8 Mon Feb 24 05:43:54 2020

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz  
2 "physical id"s (chips)  
96 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 24  
siblings : 48  
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29  
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 96  
On-line CPU(s) list: 0-95  
Thread(s) per core: 2  
Core(s) per socket: 24  
Socket(s): 2  
NUMA node(s): 4

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Platform Notes (Continued)

```

Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,48-51,55-57,61-63,67,68
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92
NUMA node3 CPU(s): 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 36608 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
node 0 size: 192102 MB
node 0 free: 178666 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
node 1 size: 193526 MB
node 1 free: 183589 MB
node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
node 2 size: 193497 MB
node 2 free: 183685 MB
node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Platform Notes (Continued)

```
node 3 size: 193523 MB
node 3 free: 183663 MB
node distances:
node  0  1  2  3
  0:  10  11  21  21
  1:  11  10  21  21
  2:  21  21  10  11
  3:  21  21  11  10
```

```
From /proc/meminfo
MemTotal:          791192876 kB
HugePages_Total:      0
Hugepagesize:       2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-4lf8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

#### Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault):          No status reported
Microarchitectural Data Sampling:          No status reported
CVE-2017-5754 (Meltdown):                  Not affected
CVE-2018-3639 (Speculative Store Bypass):  Mitigation: Speculative Store Bypass disabled
                                              via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):          Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):          Mitigation: Indirect Branch Restricted
                                              Speculation, IBPB, IBRS_FW
```

```
run-level 3 Feb 23 20:54
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type      Size      Used Avail Use% Mounted on
/dev/sddl       btrfs    559G      49G  510G   9% /home
```

```
From /sys/devices/virtual/dmi/id
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

### Platform Notes (Continued)

BIOS: Cisco Systems, Inc. C220M5.4.0.4i.0.0831191119 08/31/2019

Vendor: Cisco Systems Inc

Product: UCSC-C220-M5SX

Serial: WZP22380Z2S

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

### Compiler Version Notes

```
=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
-----
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
=====
C++       | 508.namd_r(base, peak) 510.parest_r(base, peak)
-----
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
=====
C++, C   | 511.povray_r(base, peak) 526.blender_r(base, peak)
-----
```

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
-----
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Compiler Version Notes (Continued)

```
-----
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran          | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                  | 554.roms_r(base, peak)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

## Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 6240R,  
2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Base Compiler Invocation (Continued)

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

## Base Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

C++ benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

(Continued on next page)





# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 6240R,  
2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Base Optimization Flags (Continued)

Benchmarks using both C and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R, 2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

538.imagick\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab\_r: Same as 538.imagick\_r

C++ benchmarks:

508.namd\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

510.parest\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte

549.fotonik3d\_r: Same as 503.bwaves\_r

554.roms\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

Benchmarks using both C and C++:

511.povray\_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

526.blender\_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)



# SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6240R,  
2.40GHz)

SPECrate®2017\_fp\_base = 246

SPECrate®2017\_fp\_peak = 249

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Feb-2020

**Hardware Availability:** Feb-2020

**Software Availability:** May-2019

## Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):

```
-ffinite-math-only -qopt-mem-layout-trans=4 -auto  
-nostandard-realloc-lhs -align array32byte
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-24 05:43:54-0500.

Report generated on 2020-03-17 16:22:42 by CPU2017 PDF formatter v6255.

Originally published on 2020-03-17.