



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Hewlett Packard Enterprise

(Test Sponsor: HPE)

### Synergy 480 Gen10

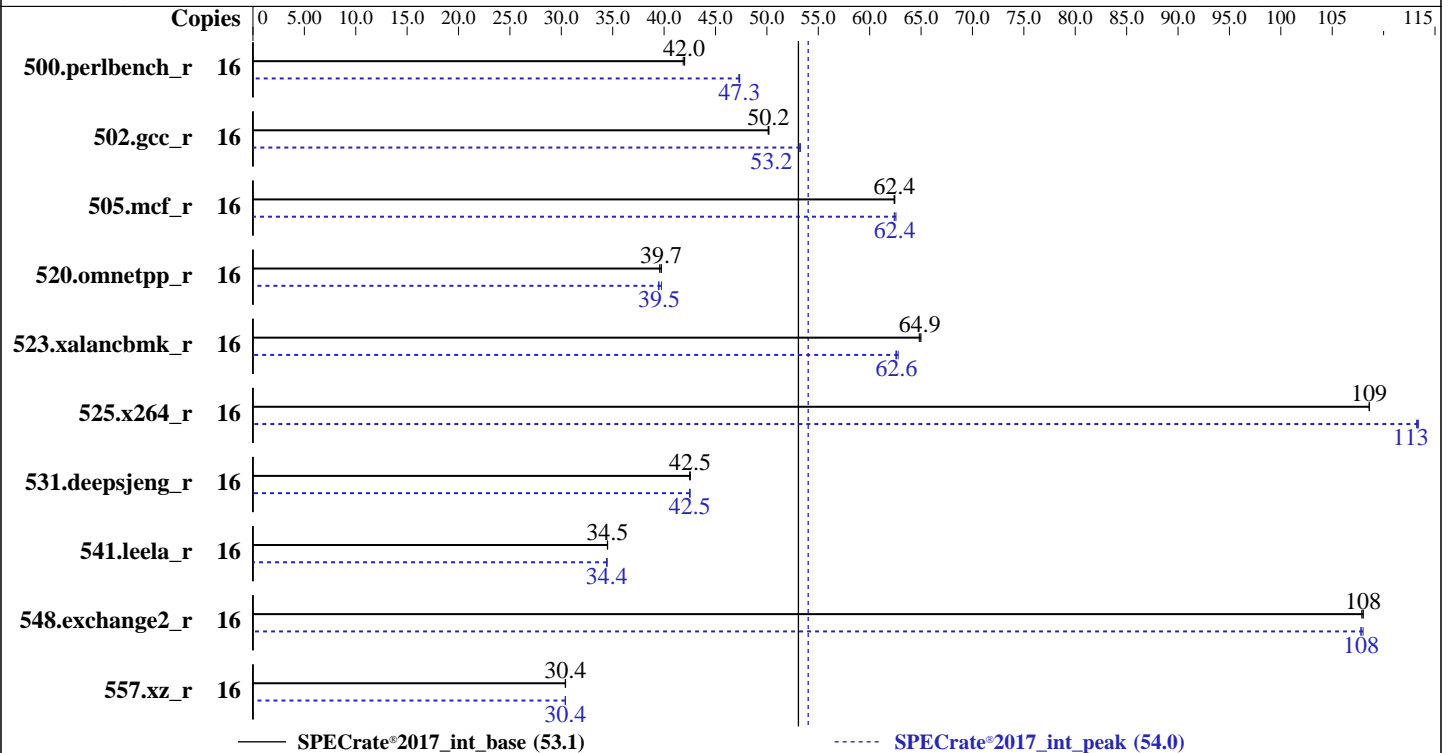
(1.90 GHz, Intel Xeon Bronze 3206R)

## SPECrate®2017\_int\_base = 53.1

## SPECrate®2017\_int\_peak = 54.0

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019



### Hardware

CPU Name: Intel Xeon Bronze 3206R  
Max MHz: 1900  
Nominal: 1900  
Enabled: 16 cores, 2 chips  
Orderable: 1, 2 chip(s)  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 11 MB I+D on chip per chip  
Other: None  
Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)  
Storage: 1 x 400 GB SAS SSD, RAID 0  
Other: None

### Software

OS: SUSE Linux Enterprise Server 15 SP1 (x86\_64)  
Kernel 4.12.14-195-default  
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++  
Compiler Build 20190416 for Linux;  
Fortran: Version 19.0.4.227 of Intel Fortran  
Compiler Build 20190416 for Linux;  
Parallel: No  
Firmware: HPE BIOS Version I42 v2.22 (11/13/2019) released Apr-2020  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 32/64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

SPECrate®2017\_int\_base = 53.1

SPECrate®2017\_int\_peak = 54.0

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019

## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	16	<b>607</b>	<b>42.0</b>	606	42.0	609	41.9	16	538	47.4	<b>538</b>	<b>47.3</b>	539	47.3
502.gcc_r	16	<b>452</b>	<b>50.2</b>	451	50.2	452	50.1	16	425	53.3	426	53.2	<b>426</b>	<b>53.2</b>
505.mcf_r	16	415	62.4	414	62.4	<b>414</b>	<b>62.4</b>	16	413	62.6	414	62.4	<b>414</b>	<b>62.4</b>
520.omnetpp_r	16	528	39.7	531	39.6	<b>529</b>	<b>39.7</b>	16	532	39.5	<b>531</b>	<b>39.5</b>	528	39.7
523.xalancbmk_r	16	260	65.0	261	64.8	<b>260</b>	<b>64.9</b>	16	270	62.5	269	62.8	<b>270</b>	<b>62.6</b>
525.x264_r	16	258	109	258	109	<b>258</b>	<b>109</b>	16	247	113	<b>247</b>	<b>113</b>	247	113
531.deepsjeng_r	16	431	42.5	<b>431</b>	<b>42.5</b>	431	42.5	16	432	42.5	<b>431</b>	<b>42.5</b>	431	42.5
541.leela_r	16	768	34.5	<b>768</b>	<b>34.5</b>	768	34.5	16	769	34.4	<b>770</b>	<b>34.4</b>	770	34.4
548.exchange2_r	16	<b>388</b>	<b>108</b>	389	108	388	108	16	388	108	389	108	<b>389</b>	<b>108</b>
557.xz_r	16	568	30.4	<b>568</b>	<b>30.4</b>	569	30.4	16	<b>568</b>	<b>30.4</b>	569	30.4	568	30.4

SPECrate®2017\_int\_base = **53.1**

SPECrate®2017\_int\_peak = **54.0**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3 > /proc/sys/vm/drop\_caches

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH =  
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

## General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Configuration:

Thermal Configuration set to Maximum Cooling

Memory Patrol Scrubbing set to Disabled

LLC Prefetch set to Enabled

LLC Dead Line Allocation set to Disabled

Enhanced Processor Performance set to Enabled

Workload Profile set to General Throughput Compute

Workload Profile set to Custom

Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011

running on sy480-sys2 Tue Mar 24 10:55:50 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz

2 "physical id"s (chips)

16 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 8

siblings : 8

physical 0: cores 0 1 2 3 4 5 6 7

physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

Address sizes: 46 bits physical, 48 bits virtual

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019

## Platform Notes (Continued)

```

CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping: 7
CPU MHz: 1900.000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-3,8-11
NUMA node1 CPU(s): 4-7,12-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx fl6c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local dtherm arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 11264 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 8 9 10 11
node 0 size: 193057 MB
node 0 free: 192594 MB
node 1 cpus: 4 5 6 7 12 13 14 15
node 1 size: 193307 MB
node 1 free: 193020 MB
node distances:
node  0  1

```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019

## Platform Notes (Continued)

```
0: 10 21
1: 21 10
```

```
From /proc/meminfo
MemTotal:      395637872 kB
HugePages_Total:      0
Hugepagesize:    2048 kB
```

```
From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"
```

```
uname -a:
Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-3620 (L1 Terminal Fault):      Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):      Mitigation: Enhanced IBRS, IBPB: conditional,
RSB filling
```

```
run-level 3 Mar 24 10:53
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type      Size      Used Avail Use% Mounted on
/dev/sda2        btrfs    371G    122G   248G   33% /home
```

```
From /sys/devices/virtual/dmi/id
BIOS:      HPE I42 11/13/2019
Vendor:    HPE
Product:   Synergy 480 Gen10
Product Family: Synergy
Serial:    MXQ72204FC
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10

(1.90 GHz, Intel Xeon Bronze 3206R)

SPECrate®2017\_int\_base = 53.1

SPECrate®2017\_int\_peak = 54.0

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

## Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

## Compiler Version Notes

=====  
C | 502.gcc\_r(peak)  
-----

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 502.gcc\_r(peak)  
-----

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C | 500.perlbench\_r(base, peak) 502.gcc\_r(base) 505.mcf\_r(base, peak)  
525.x264\_r(base, peak) 557.xz\_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----  
=====

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10

(1.90 GHz, Intel Xeon Bronze 3206R)

SPECrate®2017\_int\_base = 53.1

SPECrate®2017\_int\_peak = 54.0

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Mar-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Jun-2019

## Compiler Version Notes (Continued)

C++ | 523.xalancbmk\_r(peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)  
531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 523.xalancbmk\_r(peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version  
19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
C++ | 520.omnetpp\_r(base, peak) 523.xalancbmk\_r(base)  
531.deepsjeng\_r(base, peak) 541.leela\_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 548.exchange2\_r(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10

(1.90 GHz, Intel Xeon Bronze 3206R)

SPECrate®2017\_int\_base = 53.1

SPECrate®2017\_int\_peak = 54.0

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

## Base Compiler Invocation (Continued)

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

502.gcc\_r: -DSPEC\_LP64

505.mcf\_r: -DSPEC\_LP64

520.omnetpp\_r: -DSPEC\_LP64

523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX

525.x264\_r: -DSPEC\_LP64

531.deepsjeng\_r: -DSPEC\_LP64

541.leela\_r: -DSPEC\_LP64

548.exchange2\_r: -DSPEC\_LP64

557.xz\_r: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte

-L/usr/local/IntelCompiler19/compilers\_and\_libraries\_2019.4.227/linux/compiler/lib/intel64

-lqkmalloc





# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc -m64 -std=c11
```

```
502 gcc_r: icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
```

```
502 gcc_r: -D_FILE_OFFSET_BITS=64
```

```
505.mcf_r: -DSPEC_LP64
```

```
520.omnetpp_r: -DSPEC_LP64
```

```
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
```

```
525.x264_r: -DSPEC_LP64
```

```
531.deepsjeng_r: -DSPEC_LP64
```

```
541.leela_r: -DSPEC_LP64
```

```
548.exchange2_r: -DSPEC_LP64
```

```
557.xz_r: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
500.perlbench_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
```

```
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-fno-strict-overflow
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
```

```
-lqkmalloc
```

```
502 gcc_r: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
```

```
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```
505.mcf_r: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=4
```

(Continued on next page)



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

## Peak Optimization Flags (Continued)

505.mcf\_r (continued):

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

525.x264\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

```
-qopt-mem-layout-trans=4 -fno-alias
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

557.xz\_r: Same as 505.mcf\_r

C++ benchmarks:

520.omnetpp\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

```
-qopt-mem-layout-trans=4
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

523.xalancbmk\_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo

```
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
```

```
-L/usr/local/je5.0.1-32/lib -ljemallocc
```

531.deepsjeng\_r: Same as 520.omnetpp\_r

541.leela\_r: Same as 520.omnetpp\_r

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

```
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
```

```
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmallocc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html>

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml>

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10**

(1.90 GHz, Intel Xeon Bronze 3206R)

**SPECrate®2017\_int\_base = 53.1**

**SPECrate®2017\_int\_peak = 54.0**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Mar-2020

**Hardware Availability:** Apr-2020

**Software Availability:** Jun-2019

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-24 10:55:49-0400.

Report generated on 2020-04-28 15:30:41 by CPU2017 PDF formatter v6255.

Originally published on 2020-04-28.