



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise

(Test Sponsor: HPE)

ProLiant DL110 Gen10 Plus

(2.30 GHz, Intel Xeon Gold 6314U)

SPECrate®2017_fp_base = 209

SPECrate®2017_fp_peak = 221

CPU2017 License: 3

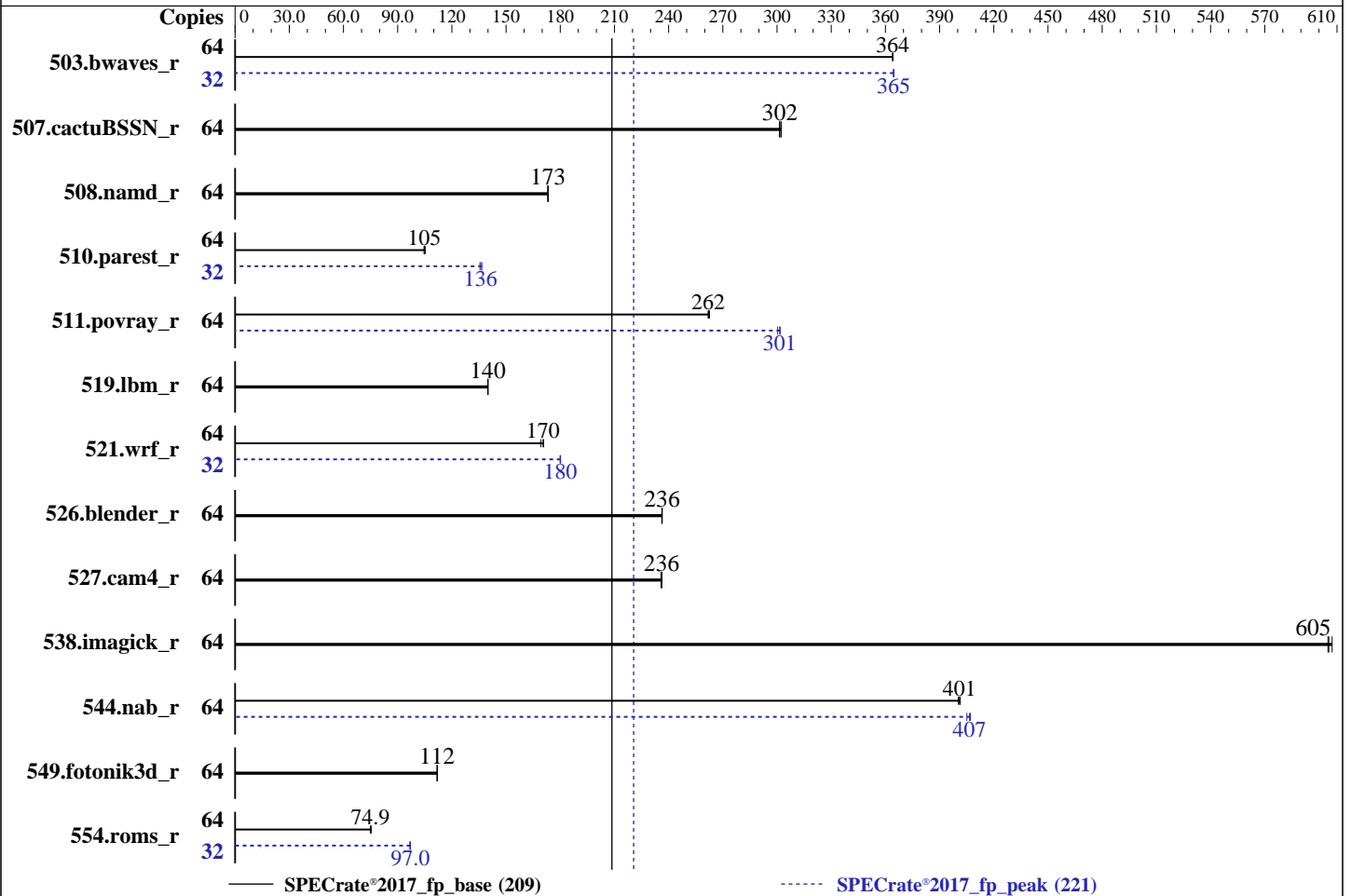
Test Sponsor: HPE

Tested by: HPE

Test Date: Jun-2021

Hardware Availability: Jun-2021

Software Availability: Jun-2021



Hardware

CPU Name: Intel Xeon Gold 6314U
 Max MHz: 3400
 Nominal: 2300
 Enabled: 32 cores, 1 chip, 2 threads/core
 Orderable: 1 chip
 Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 48 MB I+D on chip per chip
 Other: None
 Memory: 512 GB (8 x 64 GB 2Rx4 PC4-3200AA-R)
 Storage: 1 x 480 GB NVMe SSD, RAID 0
 Other: None

Software

OS: Red Hat Enterprise Linux 8.3 (Ootpa)
 Kernel 4.18.0-240.el8.x86_64
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
 Parallel: No
 Firmware: HPE BIOS Version U56 v1.50 05/13/2021 released May-2021
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
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Software (Continued)

Power Management: BIOS set to prefer performance at the cost of additional power usage

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	64	1763	364	<u>1763</u>	<u>364</u>	1763	364	32	<u>880</u>	<u>365</u>	880	364	880	365
507.cactuBSSN_r	64	269	301	<u>269</u>	<u>302</u>	268	302	64	269	301	<u>269</u>	<u>302</u>	268	302
508.namd_r	64	<u>351</u>	<u>173</u>	351	173	351	173	64	<u>351</u>	<u>173</u>	351	173	351	173
510.parest_r	64	<u>1597</u>	<u>105</u>	1591	105	1601	105	32	<u>616</u>	<u>136</u>	613	137	618	136
511.povray_r	64	<u>570</u>	<u>262</u>	569	263	571	262	64	498	300	<u>496</u>	<u>301</u>	495	302
519.lbm_r	64	482	140	482	140	<u>482</u>	<u>140</u>	64	482	140	482	140	<u>482</u>	<u>140</u>
521.wrf_r	64	<u>841</u>	<u>170</u>	847	169	839	171	32	<u>398</u>	<u>180</u>	398	180	398	180
526.blender_r	64	413	236	<u>412</u>	<u>236</u>	412	236	64	413	236	<u>412</u>	<u>236</u>	412	236
527.cam4_r	64	475	236	<u>474</u>	<u>236</u>	474	236	64	475	236	<u>474</u>	<u>236</u>	474	236
538.imagick_r	64	263	605	<u>263</u>	<u>605</u>	262	607	64	263	605	<u>263</u>	<u>605</u>	262	607
544.nab_r	64	268	401	<u>269</u>	<u>401</u>	269	400	64	266	405	<u>265</u>	<u>407</u>	265	407
549.fotonik3d_r	64	2229	112	<u>2229</u>	<u>112</u>	2230	112	64	2229	112	<u>2229</u>	<u>112</u>	2230	112
554.roms_r	64	1358	74.9	1347	75.5	<u>1357</u>	<u>74.9</u>	32	524	97.0	<u>524</u>	<u>97.0</u>	525	96.8

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/cpu2017/lib/intel64:/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"



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General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1

runcpu command invoked through numactl i.e.:

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Submitted_by: "Bhatnagar, Prateek" <prateek.bhatnagar@hpe.com>

Submitted: Mon Jun 21 10:17:01 EDT 2021

Submission: cpu2017-20210621-27519.sub

Platform Notes

The system ROM used for this result contains Intel microcode version 0xd0002a0 for the Intel Xeon Gold 6314U processor.

BIOS Configuration:

Workload Profile set to General Throughput Compute

Memory Patrol Scrubbing set to Disabled

Advanced Memory Protection set to Advanced ECC

Last Level Cache (LLC) Prefetch set to Enabled

Last Level Cache (LLC) Dead Line Allocation set to Disabled

Enhanced Processor Performance set to Enabled

Enhanced Processor Performance Profile set to Aggressive

Thermal Configuration set to Maximum Cooling

Workload Profile set to Custom

DCU Stream Prefetcher set to Disabled

XPT Remote Prefetcher set to Enabled

Energy/Performance Bias set to Balanced Performance

Sysinfo program /cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost.localdomain Wed Jun 16 04:38:20 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6314U CPU @ 2.30GHz

(Continued on next page)



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Platform Notes (Continued)

1 "physical id"s (chips)

64 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 32

siblings : 64

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31

From lscpu from util-linux 2.32.1:

Architecture: x86_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 64

On-line CPU(s) list: 0-63

Thread(s) per core: 2

Core(s) per socket: 32

Socket(s): 1

NUMA node(s): 2

Vendor ID: GenuineIntel

CPU family: 6

Model: 106

Model name: Intel(R) Xeon(R) Gold 6314U CPU @ 2.30GHz

Stepping: 6

CPU MHz: 1659.267

BogoMIPS: 4600.00

Virtualization: VT-x

L1d cache: 48K

L1i cache: 32K

L2 cache: 1280K

L3 cache: 49152K

NUMA node0 CPU(s): 0-15,32-47

NUMA node1 CPU(s): 16-31,48-63

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq
rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw
avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts avx512vbmi umip pku
ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme
avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

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Platform Notes (Continued)

```
/proc/cpuinfo cache data
cache size : 49152 KB
```

```
From numactl --hardware
```

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```
available: 2 nodes (0-1)
```

```
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
44 45 46 47
```

```
node 0 size: 248656 MB
```

```
node 0 free: 256927 MB
```

```
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63
```

```
node 1 size: 249278 MB
```

```
node 1 free: 256651 MB
```

```
node distances:
```

```
node 0 1
```

```
0: 10 20
```

```
1: 20 10
```

```
From /proc/meminfo
```

```
MemTotal: 528044728 kB
```

```
HugePages_Total: 0
```

```
Hugepagesize: 2048 kB
```

```
/sbin/tuned-adm active
```

```
Current active profile: throughput-performance
```

```
From /etc/*release* /etc/*version*
```

```
os-release:
```

```
NAME="Red Hat Enterprise Linux"
```

```
VERSION="8.3 (Ootpa)"
```

```
ID="rhel"
```

```
ID_LIKE="fedora"
```

```
VERSION_ID="8.3"
```

```
PLATFORM_ID="platform:el8"
```

```
PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
```

```
ANSI_COLOR="0;31"
```

```
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
```

```
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
```

```
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga
```

```
uname -a:
```

```
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux
```

```
Kernel self-reported vulnerability status:
```

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Platform Notes (Continued)

CVE-2018-12207 (iTLB Multihit):	Not affected
CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):	Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):	Not affected
CVE-2019-11135 (TSX Asynchronous Abort):	Not affected

run-level 3 Jun 16 02:51

SPEC is set to: /cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/nvme1n1p4	xf	442G	144G	298G	33%	/

From /sys/devices/virtual/dmi/id

Vendor:	HPE
Product:	ProLiant DL110 Gen10 Plus
Product Family:	ProLiant
Serial:	T912PP0032

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

8x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200

BIOS:

BIOS Vendor:	HPE
BIOS Version:	U56
BIOS Date:	05/13/2021
BIOS Revision:	1.50
Firmware Revision:	2.40

(End of data from sysinfo program)



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Compiler Version Notes

```
=====
C                | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                  | 544.nab_r(base, peak)
=====
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

```
=====
C++              | 508.namd_r(base, peak) 510.parest_r(base, peak)
=====
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C           | 511.povray_r(peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C           | 511.povray_r(base) 526.blender_r(base, peak)
=====
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

```
=====
C++, C           | 511.povray_r(peak)
=====
```

```
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
=====
```

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Compiler Version Notes (Continued)

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=====
C++, C | 511.povray_r(base) 526.blender_r(base, peak)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000

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=====
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====
Fortran, C | 521.wrf_r(peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000

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Compiler Version Notes (Continued)

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

=====
Fortran, C | 521.wrf_r(peak)
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
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=====

=====
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)
=====

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

(Continued on next page)



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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

ifort icx

Benchmarks using both C and C++:

icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifort

Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
```

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SPECrate®2017_fp_base = 209

SPECrate®2017_fp_peak = 221

CPU2017 License: 3

Test Sponsor: HPE

Tested by: HPE

Test Date: Jun-2021

Hardware Availability: Jun-2021

Software Availability: Jun-2021

Base Optimization Flags (Continued)

Fortran benchmarks (continued):

```
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using both Fortran and C:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using both C and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using Fortran, C, and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

Peak Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

521.wrf_r: ifort icc

(Continued on next page)



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Peak Compiler Invocation (Continued)

527.cam4_r: ifort icx

Benchmarks using both C and C++:

511.povray_r: icpc icc

526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:

503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only

(Continued on next page)



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Peak Optimization Flags (Continued)

503.bwaves_r (continued):

```
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-ljmalloc -L/usr/local/jemalloc64-5.0.1/lib
```

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

```
521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-nostandard-realloc-lhs -align array32byte -auto  
-L/usr/local/jemalloc64-5.0.1/lib -ljmalloc
```

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljmalloc
```

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.html>

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.xml>

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml



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