



# SPEC CPU®2017 Floating Point Rate Result

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## Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DIT400TR-436R  
(2.10 GHz, Intel Xeon Silver 4216)

SPECrate®2017\_fp\_base = 185

SPECrate®2017\_fp\_peak = 186

CPU2017 License: 006042

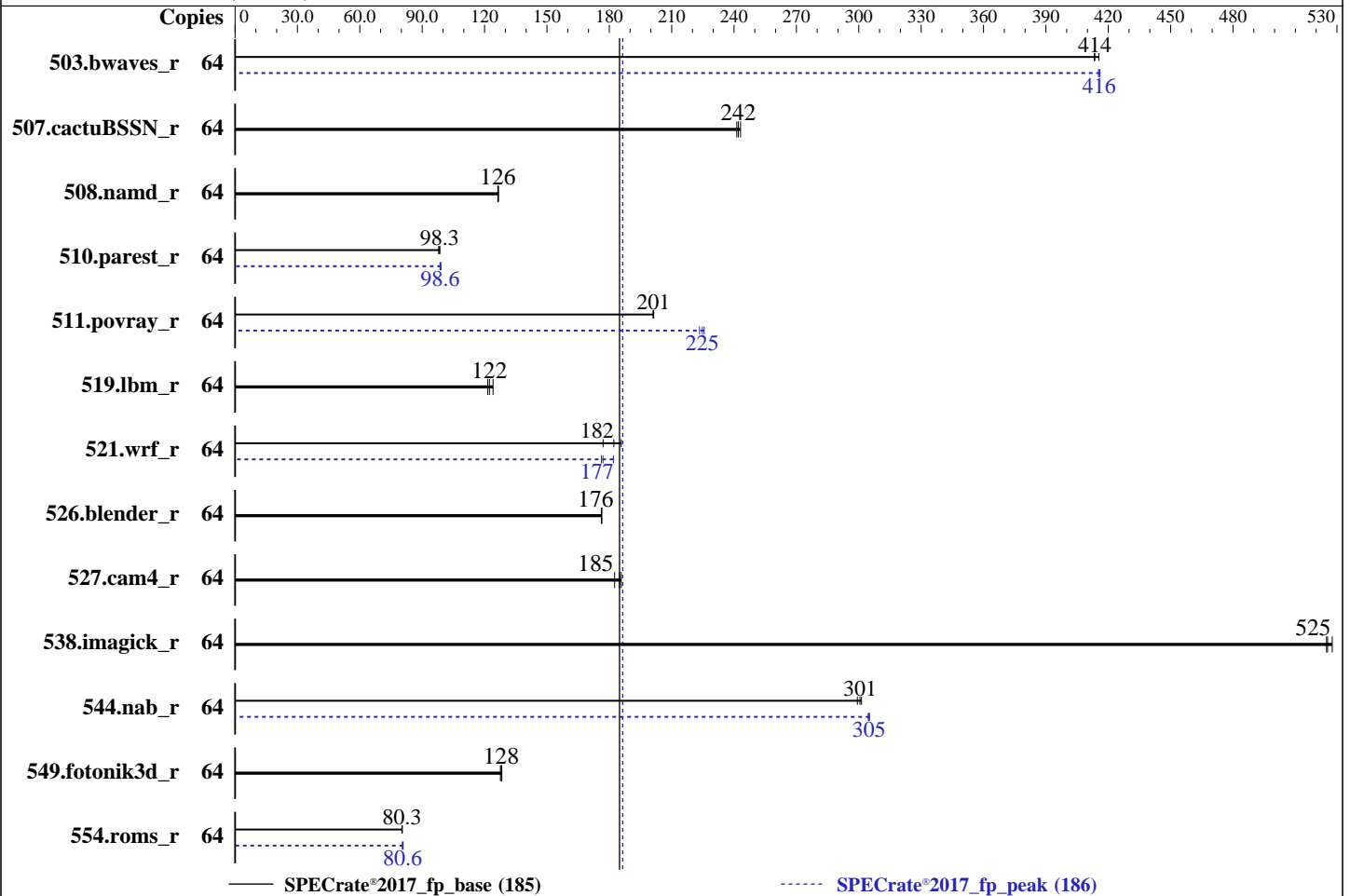
Test Sponsor: Netweb Pte Ltd

Tested by: Tyrone Systems

Test Date: Aug-2021

Hardware Availability: Apr-2019

Software Availability: Jul-2021



### Hardware

CPU Name: Intel Xeon Silver 4216  
 Max MHz: 3200  
 Nominal: 2100  
 Enabled: 32 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 Chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 22 MB I+D on chip per chip  
 Other: None  
 Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)  
 Storage: 1 x 480 GB SATA SSD  
 Other: None

### Software

OS: CentOS Linux release 8.4.2105  
 Kernel 4.18.0-305.3.1.el8.x86\_64  
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
 Parallel: No  
 Firmware: Version V8.104 released Jul-2021  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	64	<b>1552</b>	<b>414</b>	1553	413	1545	415	64	1543	416	<b>1544</b>	<b>416</b>	1545	415
507.cactuBSSN_r	64	<b>335</b>	<b>242</b>	333	243	336	241	64	<b>335</b>	<b>242</b>	333	243	336	241
508.namd_r	64	480	127	<b>481</b>	<b>126</b>	481	126	64	480	127	<b>481</b>	<b>126</b>	481	126
510.parest_r	64	<b>1702</b>	<b>98.3</b>	1711	97.9	1700	98.5	64	<b>1697</b>	<b>98.6</b>	1690	99.0	1698	98.6
511.povray_r	64	<b>743</b>	<b>201</b>	743	201	742	201	64	662	226	669	223	<b>665</b>	<b>225</b>
519.lbm_r	64	544	124	<b>551</b>	<b>122</b>	555	122	64	544	124	<b>551</b>	<b>122</b>	555	122
521.wrf_r	64	810	177	<b>787</b>	<b>182</b>	772	186	64	788	182	<b>810</b>	<b>177</b>	814	176
526.blender_r	64	553	176	553	176	<b>553</b>	<b>176</b>	64	553	176	553	176	<b>553</b>	<b>176</b>
527.cam4_r	64	613	183	603	186	<b>606</b>	<b>185</b>	64	613	183	603	186	<b>606</b>	<b>185</b>
538.imagick_r	64	<b>303</b>	<b>525</b>	303	525	302	528	64	<b>303</b>	<b>525</b>	303	525	302	528
544.nab_r	64	<b>358</b>	<b>301</b>	357	301	360	299	64	353	305	354	305	<b>353</b>	<b>305</b>
549.fotonik3d_r	64	<b>1948</b>	<b>128</b>	1954	128	1944	128	64	<b>1948</b>	<b>128</b>	1954	128	1944	128
554.roms_r	64	1267	80.2	1264	80.4	<b>1266</b>	<b>80.3</b>	64	<b>1262</b>	<b>80.6</b>	1264	80.5	1258	80.8

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SPECrate®2017\_fp\_peak = 186

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOC\_CONF = "retain:true"

## General Notes

Binaries compiled locally by Netweb  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:

(Continued on next page)



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## General Notes (Continued)

```
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Settings:

Power Technology set to Custom

Power Performance Tuning set to BIOS Controls EPB

ENERGY\_PERF\_BIAS\_CFG mode set to Performance

LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on spec Thu Aug 12 14:05:58 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
```

```
2 "physical id"s (chips)
```

```
64 "processors"
```

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 16
```

```
siblings : 32
```

```
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

```
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu from util-linux 2.32.1:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 64

On-line CPU(s) list: 0-63

Thread(s) per core: 2

(Continued on next page)



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## Platform Notes (Continued)

```

Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
BIOS Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 7
CPU MHz: 800.086
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15,32-47
NUMA node1 CPU(s): 16-31,48-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req pku ospke avx512_vnni md_clear flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 22528 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)

```

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43
44 45 46 47

```

node 0 size: 192069 MB

node 0 free: 175720 MB

```

node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63

```

node 1 size: 193528 MB

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## Platform Notes (Continued)

node 1 free: 179158 MB

node distances:

```

node  0  1
   0: 10 21
   1: 21 10

```

From /proc/meminfo

```

MemTotal:      394851996 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

/sbin/tuned-adm active

Current active profile: throughput-performance

/sys/devices/system/cpu/cpu\*/cpufreq/scaling\_governor has performance

From /etc/\*release\* /etc/\*version\*

```

centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
  NAME="CentOS Linux"
  VERSION="8"
  ID="centos"
  ID_LIKE="rhel fedora"
  VERSION_ID="8"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="CentOS Linux 8"
  ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

```

uname -a:

```

Linux spec 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64
x86_64 GNU/Linux

```

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):	KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault):	Not affected
Microarchitectural Data Sampling:	Not affected
CVE-2017-5754 (Meltdown):	Not affected
CVE-2018-3639 (Speculative Store Bypass):	Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):	Mitigation: usercopy/swapgs

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## Platform Notes (Continued)

```

barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: TSX disabled

run-level 3 Aug 12 05:10

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/mapper/cl-home xfs   372G  198G  174G  54% /home

From /sys/devices/virtual/dmi/id
Vendor:          Tyrone Systems
Product:         Tyrone Camarero DIT400TR-436R
Product Family: empty
Serial:         empty

Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
  12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:
  BIOS Vendor:    American Megatrends Inc.
  BIOS Version:   V8.104
  BIOS Date:      07/27/2021
  BIOS Revision:  5.14
  Firmware Revision: 6.1

(End of data from sysinfo program)

```

## Compiler Version Notes

```

=====
C          | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
          | 544.nab_r(base, peak)
=====

```

```

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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=====

```

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## Compiler Version Notes (Continued)

=====  
C++ | 508.namd\_r(base, peak) 510.parest\_r(base, peak)  
-----

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base, peak)  
-----

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(peak)  
-----

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C++, C | 511.povray\_r(base) 526.blender\_r(base, peak)  
-----

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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=====  
C++, C, Fortran | 507.cactuBSSN\_r(base, peak)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
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=====  
Fortran | 503.bwaves\_r(base, peak) 549.fotonik3d\_r(base, peak)  
| 554.roms\_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
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=====  
Fortran, C | 521.wrf\_r(peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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=====  
Fortran, C | 521.wrf\_r(peak)  
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base, peak)  
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:  
icx

C++ benchmarks:  
icpx

Fortran benchmarks:  
ifort

Benchmarks using both Fortran and C:  
ifort icx

Benchmarks using both C and C++:  
icpx icx

Benchmarks using Fortran, C, and C++:  
icpx icx ifort



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## Base Portability Flags

```

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

```

## Base Optimization Flags

C benchmarks:

```

-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

```

C++ benchmarks:

```

-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

```

Fortran benchmarks:

```

-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

```

Benchmarks using both Fortran and C:

```

-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib

```

Benchmarks using both C and C++:

```

-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

```

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# SPEC CPU®2017 Floating Point Rate Result

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**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DIT400TR-436R  
(2.10 GHz, Intel Xeon Silver 4216)

SPECrate®2017\_fp\_base = 185

SPECrate®2017\_fp\_peak = 186

**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2019  
**Software Availability:** Jul-2021

## Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):

```
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib
```

Benchmarks using Fortran, C, and C++:

```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib
```

## Peak Compiler Invocation

C benchmarks:

```
icx
```

C++ benchmarks:

```
icpx
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
521.wrf_r: ifort icc
```

```
527.cam4_r: ifort icx
```

Benchmarks using both C and C++:

```
511.povray_r: icpc icc
```

```
526.blender_r: icpx icx
```

Benchmarks using Fortran, C, and C++:

```
icpx icx ifort
```

## Peak Portability Flags

Same as Base Portability Flags



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**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Tested by:** Tyrone Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2019

**Software Availability:** Jul-2021

## Peak Optimization Flags

C benchmarks:

519.lbm\_r: basepeak = yes

538.imagick\_r: basepeak = yes

544.nab\_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto  
-Ofast -qopt-mem-layout-trans=4  
-fimf-accuracy-bits=14:sqrt  
-mbranches-within-32B-boundaries -ljemalloc  
-L/usr/local/je5.0.1-64/lib

C++ benchmarks:

508.namd\_r: basepeak = yes

510.parest\_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math  
-flto -mfpmath=sse -funroll-loops  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:

503.bwaves\_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-ljemalloc -L/usr/local/je5.0.1-64/lib

549.fotonik3d\_r: basepeak = yes

554.roms\_r: Same as 503.bwaves\_r

Benchmarks using both Fortran and C:

521.wrf\_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-nostandard-realloc-lhs -align array32byte -auto  
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4\_r: basepeak = yes

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**Tyrone Systems**

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(2.10 GHz, Intel Xeon Silver 4216)

**SPECrate®2017\_fp\_base = 185**

**SPECrate®2017\_fp\_peak = 186**

**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Tested by:** Tyrone Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2019

**Software Availability:** Jul-2021

## Peak Optimization Flags (Continued)

Benchmarks using both C and C++:

```
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3  
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-multiple-gather-scatter-by-shuffles  
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

526.blender\_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN\_r: basepeak = yes

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml>

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Tested with SPEC CPU®2017 v1.1.8 on 2021-08-12 14:05:57-0400.

Report generated on 2021-09-21 16:17:53 by CPU2017 PDF formatter v6442.

Originally published on 2021-09-21.