SPEC CPU®2017 Integer Speed Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

$SPECspeed®2017\_int\_base =$ 10.9

$SPECspeed®2017\_int\_peak =$ Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Threads — scale 0 to 20.0

Benchmark	Threads	Result
600.perlbench_s	16	7.05
602.gcc_s	16	9.92
605.mcf_s	16	19.5
620.omnetpp_s	16	6.74
623.xalancbmk_s	16	13.6
625.x264_s	16	16.7
631.deepsjeng_s	16	6.06
641.leela_s	16	5.03
648.exchange2_s	16	20.0
657.xz_s	16	19.6

——— SPECspeed®2017_int_base (10.9)

Hardware

CPU Name: Intel Xeon Silver 4309Y
 Max MHz: 3600
 Nominal: 2800
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 12 MB I+D on chip per chip
 Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
Storage: 1 x 480 GB SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base = 10.9
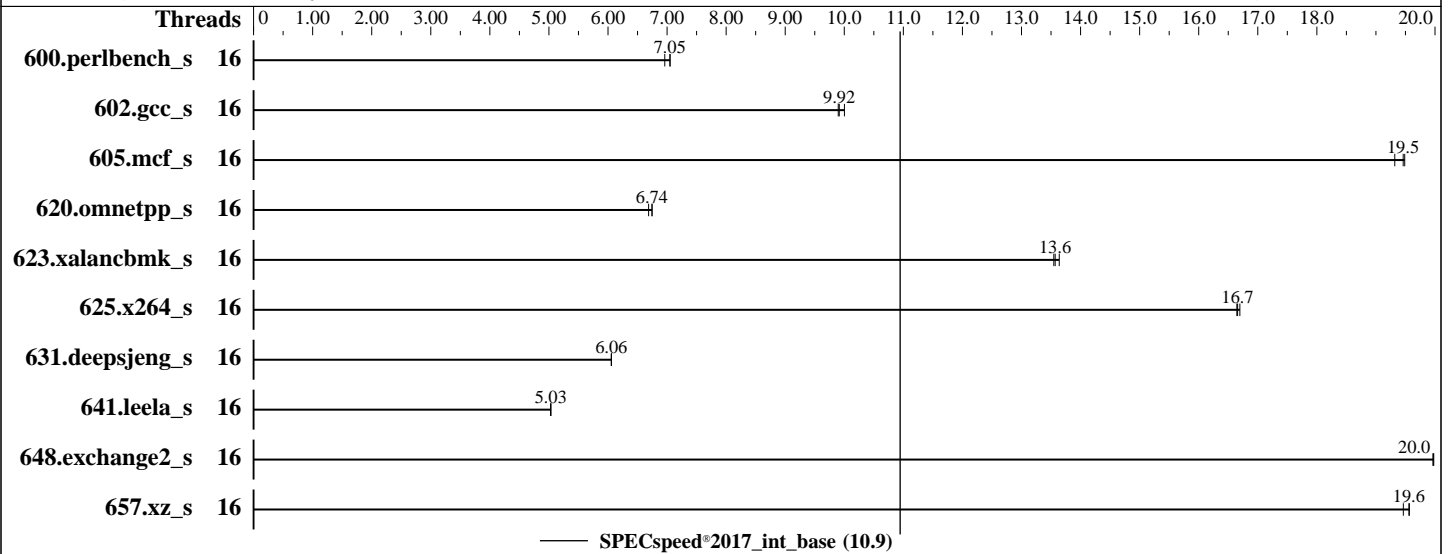
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	16	255	6.96	252	7.05	**252**	**7.05**							
602.gcc_s	16	402	9.90	**402**	**9.92**	398	10.0							
605.mcf_s	16	244	19.3	242	19.5	**243**	**19.5**							
620.omnetpp_s	16	**242**	**6.74**	242	6.75	244	6.69							
623.xalancbmk_s	16	105	13.5	104	13.6	**104**	**13.6**							
625.x264_s	16	106	16.6	**106**	**16.7**	106	16.7							
631.deepsjeng_s	16	**237**	**6.06**	237	6.06	237	6.06							
641.leela_s	16	339	5.03	**339**	**5.03**	339	5.03							
648.exchange2_s	16	147	20.0	**147**	**20.0**	147	20.0							
657.xz_s	16	316	19.6	**316**	**19.6**	318	19.5							
SPECspeed®2017_int_base =	**10.9**													
SPECspeed®2017_int_peak =	**Not Run**													

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

$SPECspeed^{®}2017\_int\_base =$ 10.9

$SPECspeed^{®}2017_int_peak = $ Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

```
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on install Sat Aug 21 12:22:19 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
       2  "physical id"s (chips)
       16 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 8
       siblings  : 8
       physical 0: cores 0 1 2 3 4 5 6 7
       physical 1: cores 0 1 2 3 4 5 6 7

 From lscpu from util-linux 2.33.1:
    Architecture:        x86_64
    CPU op-mode(s):      32-bit, 64-bit
    Byte Order:          Little Endian
```

(Continued on next page)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base =   10.9

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

```
        Address sizes:         46 bits physical, 57 bits virtual
        CPU(s):                16
        On-line CPU(s) list:   0-15
        Thread(s) per core:    1
        Core(s) per socket:    8
        Socket(s):             2
        NUMA node(s):          2
        Vendor ID:             GenuineIntel
        CPU family:            6
        Model:                 106
        Model name:            Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
        Stepping:              6
        CPU MHz:               3387.395
        CPU max MHz:           3600.0000
        CPU min MHz:           800.0000
        BogoMIPS:              5600.00
        Virtualization:        VT-x
        L1d cache:             48K
        L1i cache:             32K
        L2 cache:              1280K
        L3 cache:              12288K
        NUMA node0 CPU(s):     0-7
        NUMA node1 CPU(s):     8-15
        Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
        pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
        lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
        aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
        xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
        avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
        mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
        fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
        avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
        avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
        cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
        hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
        avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
        arch_capabilities

 /proc/cpuinfo cache data
    cache size : 12288 KB

 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7
   node 0 size: 1031590 MB
   node 0 free: 1031197 MB
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base =   10.9

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

```
   node 1 cpus: 8 9 10 11 12 13 14 15
   node 1 size: 1032186 MB
   node 1 free: 1031679 MB
   node distances:
   node   0   1
     0:  10  20
     1:  20  10

From /proc/meminfo
   MemTotal:       2113307900 kB
   HugePages_Total:        0
   Hugepagesize:        2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
   performance

From /etc/*release* /etc/*version*
   os-release:
       NAME="SLES"
       VERSION="15-SP2"
       VERSION_ID="15.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
       ID="sles"
       ID_LIKE="suse"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
   Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
   x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                  Not affected
CVE-2018-3620 (L1 Terminal Fault):               Not affected
Microarchitectural Data Sampling:                Not affected
CVE-2017-5754 (Meltdown):                        Not affected
CVE-2018-3639 (Speculative Store Bypass):        Mitigation: Speculative Store
                                                 Bypass disabled via prctl and
                                                 seccomp
CVE-2017-5753 (Spectre variant 1):               Mitigation: usercopy/swapgs
                                                 barriers and __user pointer
                                                 sanitization
CVE-2017-5715 (Spectre variant 2):               Mitigation: Enhanced IBRS, IBPB:
                                                 conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):         Not affected
```

(Continued on next page)

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

$SPECspeed®2017\_int\_base =$ 10.9

$SPECspeed®2017\_int\_peak =$ Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

```
 run-level 3 Aug 21 12:19

 SPEC is set to: /home/cpu2017
    Filesystem      Type   Size  Used Avail Use% Mounted on
    /dev/sda4       btrfs  445G   16G  428G   4% /home

 From /sys/devices/virtual/dmi/id
    Vendor:          Cisco Systems Inc
    Product:         UCSB-B200-M6
    Serial:          FCH24097576

 Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
 interpret this section. The 'dmidecode' program reads system data which is "intended to
 allow hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

 BIOS:
    BIOS Vendor:      Cisco Systems, Inc.
    BIOS Version:     B200M6.4.2.1d.0.0730210924
    BIOS Date:        07/30/2021
    BIOS Revision:    5.22

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C         | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
          | 625.x264_s(base) 657.xz_s(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++       | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
          | 641.leela_s(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
```

(Continued on next page)

SPEC CPU®2017 Integer Speed Result

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base =   10.9

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

```
==============================================================================
Fortran | 648.exchange2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base =   10.9

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

C++ benchmarks:
```
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc
```

Fortran benchmarks:
```
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
```

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revG.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-21 12:22:19-0400.
Report generated on 2021-09-14 19:19:49 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-14.