



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

## Hewlett Packard Enterprise

(Test Sponsor: HPE)

### Synergy 480 Gen10 Plus

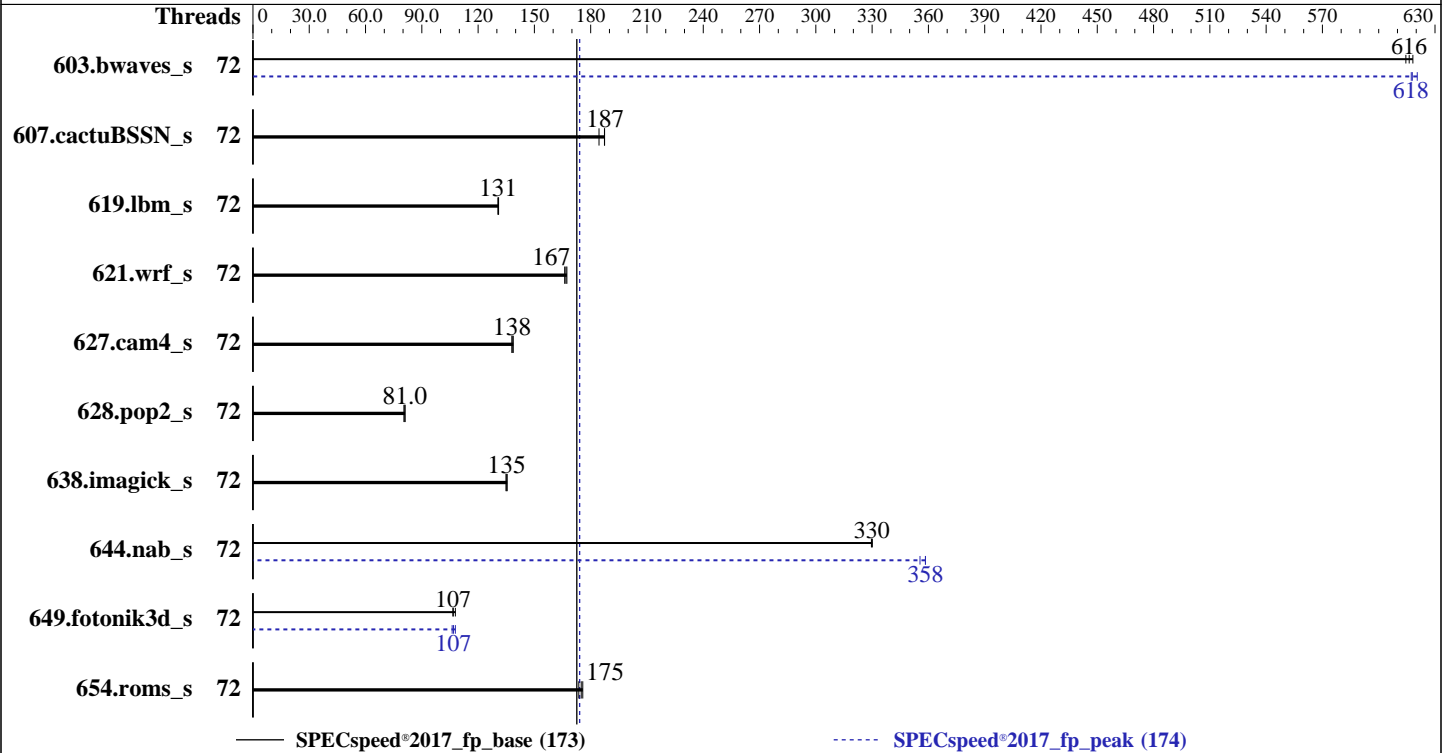
(3.00 GHz, Intel Xeon Gold 6354)

SPECspeed®2017\_fp\_base = 173

SPECspeed®2017\_fp\_peak = 174

CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE

Test Date: Dec-2021  
Hardware Availability: Nov-2021  
Software Availability: Dec-2020



### Hardware

CPU Name: Intel Xeon Gold 6354  
 Max MHz: 3600  
 Nominal: 3000  
 Enabled: 36 cores, 2 chips, 2 threads/core  
 Orderable: 1, 2 chip(s)  
 Cache L1: 32 KB I + 48 KB D on chip per core  
 L2: 1.25 MB I+D on chip per core  
 L3: 39 MB I+D on chip per chip  
 Other: None  
 Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)  
 Storage: 1 x 800 GB SAS SSD, RAID 0  
 Other: None

### Software

OS: Red Hat Enterprise Linux 8.3 (Ootpa)  
 Kernel 4.18.0-240.el8.x86\_64  
 Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
 Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
 C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
 Parallel: Yes  
 Firmware: HPE BIOS Version I44 v1.54 11/03/2021 released Nov-2021  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: 64-bit  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	72	96.0	614	95.4	618	<u>95.7</u>	<u>616</u>	72	95.1	621	<u>95.5</u>	<u>618</u>	95.6	617
607.cactuBSSN_s	72	90.4	184	<u>89.0</u>	<u>187</u>	88.9	187	72	90.4	184	<u>89.0</u>	<u>187</u>	88.9	187
619.lbm_s	72	40.0	131	40.1	131	<u>40.1</u>	<u>131</u>	72	40.0	131	40.1	131	<u>40.1</u>	<u>131</u>
621.wrf_s	72	79.6	166	79.1	167	<u>79.3</u>	<u>167</u>	72	79.6	166	79.1	167	<u>79.3</u>	<u>167</u>
627.cam4_s	72	<u>64.2</u>	<u>138</u>	63.9	139	64.2	138	72	<u>64.2</u>	<u>138</u>	63.9	139	64.2	138
628.pop2_s	72	147	81.0	<u>147</u>	<u>81.0</u>	148	80.5	72	147	81.0	<u>147</u>	<u>81.0</u>	148	80.5
638.imagick_s	72	107	135	<u>107</u>	<u>135</u>	106	135	72	107	135	<u>107</u>	<u>135</u>	106	135
644.nab_s	72	53.0	330	<u>53.0</u>	<u>330</u>	52.9	330	72	<u>48.7</u>	<u>358</u>	48.7	358	49.1	356
649.fotonik3d_s	72	85.6	107	84.5	108	<u>85.4</u>	<u>107</u>	72	85.9	106	84.5	108	<u>85.3</u>	<u>107</u>
654.roms_s	72	90.7	174	<u>90.0</u>	<u>175</u>	89.6	176	72	90.7	174	<u>90.0</u>	<u>175</u>	89.6	176

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
Tuned-adm profile was set to throughput-performance using "tuned-adm profile throughput-performance"
Cpupower Frequency was set to performance using "cpupower frequency-set -g performance"
```

## Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"
```

## General Notes

```
Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

**(3.00 GHz, Intel Xeon Gold 6354)**

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## General Notes (Continued)

jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Submitted\_by: "Bucek, James" <james.bucek@hpe.com>  
Submitted: Wed Jan 12 10:02:51 EST 2022  
Submission: cpu2017-20220103-30717.sub

## Platform Notes

BIOS Configuration:

Workload Profile set to General Peak Frequency Compute  
Thermal Configuration set to Maximum Cooling  
Memory Patrol Scrubbing set to Disabled  
Advanced Memory Protection set to Advanced ECC  
Last Level Cache (LLC) Prefetch set to Enabled  
Last Level Cache (LLC) Dead Line Allocation set to Disabled  
Enhanced Processor Performance set to Enabled  
Workload Profile set to Custom  
Energy/Performance Bias set to Balanced Power  
DCU Stream Prefetcher set to Disabled  
Adjacent Sector Prefetch set to Disabled  
Minimum Processor Idle Power Package C-State set to No Package State  
Numa Group Size Optimization set to Flat

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d  
running on localhost.localdomain Tue Dec 21 10:33:54 2021

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
 2 "physical id"s (chips)
 72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings  : 36
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
```

From lscpu from util-linux 2.32.1:  
Architecture: x86\_64

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10 Plus

(3.00 GHz, Intel Xeon Gold 6354)

SPECspeed®2017\_fp\_base = 173

SPECspeed®2017\_fp\_peak = 174

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## Platform Notes (Continued)

```

CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s):           2
NUMA node(s):       2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               106
Model name:          Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
Stepping:            6
CPU MHz:             2669.626
CPU max MHz:         3600.0000
CPU min MHz:         800.0000
BogoMIPS:            6000.00
Virtualization:     VT-x
L1d cache:           48K
L1i cache:           32K
L2 cache:            1280K
L3 cache:            39936K
NUMA node0 CPU(s):  0-17,36-53
NUMA node1 CPU(s):  18-35,54-71
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq
rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw
avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat pln pts hwp hwp_act_window
hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

```

```
/proc/cpuinfo cache data
cache size : 39936 KB
```

```
From numactl --hardware
```

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```
available: 2 nodes (0-1)
```

```
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 36 37 38 39 40 41 42 43 44 45
46 47 48 49 50 51 52 53
```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## Platform Notes (Continued)

```

node 0 size: 975867 MB
node 0 free: 1030701 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 54 55 56 57 58 59 60
61 62 63 64 65 66 67 68 69 70 71
node 1 size: 973674 MB
node 1 free: 1031628 MB
node distances:
node 0 1
  0: 10 20
  1: 20 10

From /proc/meminfo
MemTotal:      2113486628 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.3 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.3"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
  ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

uname -a:
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):      Not affected
CVE-2018-3620 (L1 Terminal Fault):   Not affected
Microarchitectural Data Sampling:   Not affected
CVE-2017-5754 (Meltdown):           Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store

```

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Dec-2021

**Hardware Availability:** Nov-2021

**Software Availability:** Dec-2020

## Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1): Bypass disabled via prctl and seccomp  
Mitigation: usercopy/swaps barriers and \_\_user pointer sanitization

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 21 10:30

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/rhel-home	xfs	670G	112G	558G	17%	/home

From /sys/devices/virtual/dmi/id

Vendor: HPE  
 Product: Synergy 480 Gen10 Plus  
 Product Family: Synergy  
 Serial: CN70330Q5F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:  
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200

BIOS:  
 BIOS Vendor: HPE  
 BIOS Version: I44  
 BIOS Date: 11/03/2021  
 BIOS Revision: 1.54  
 Firmware Revision: 2.50

(End of data from sysinfo program)

## Compiler Version Notes

```
=====
C          | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
          | 644.nab_s(base)
-----
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112\_000000

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10 Plus

(3.00 GHz, Intel Xeon Gold 6354)

SPECspeed®2017\_fp\_base = 173

SPECspeed®2017\_fp\_peak = 174

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C | 644.nab\_s(peak)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C | 619.lbm\_s(base, peak) 638.imagick\_s(base, peak)  
| 644.nab\_s(base)  
=====

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C | 644.nab\_s(peak)  
=====

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
C++, C, Fortran | 607.cactuBSSN\_s(base, peak)  
=====

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran | 603.bwaves\_s(base, peak) 649.fotonik3d\_s(base, peak)  
| 654.roms\_s(base, peak)  
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

Synergy 480 Gen10 Plus

(3.00 GHz, Intel Xeon Gold 6354)

SPECspeed®2017\_fp\_base = 173

SPECspeed®2017\_fp\_peak = 174

**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

**Test Date:** Dec-2021  
**Hardware Availability:** Nov-2021  
**Software Availability:** Dec-2020

## Compiler Version Notes (Continued)

Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=====  
Fortran, C | 621.wrf\_s(base, peak) 627.cam4\_s(base, peak)  
| 628.pop2\_s(base, peak)  
=====

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

## Base Compiler Invocation

C benchmarks:  
icc

Fortran benchmarks:  
ifort

Benchmarks using both Fortran and C:  
ifort icc

Benchmarks using Fortran, C, and C++:  
icpc icc ifort

## Base Portability Flags

603.bwaves\_s: -DSPEC\_LP64  
607.cactuBSSN\_s: -DSPEC\_LP64  
619.lbm\_s: -DSPEC\_LP64  
621.wrf\_s: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian  
627.cam4\_s: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG  
628.pop2\_s: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big\_endian  
-assume byterecl  
638.imagick\_s: -DSPEC\_LP64  
644.nab\_s: -DSPEC\_LP64  
649.fotonik3d\_s: -DSPEC\_LP64  
654.roms\_s: -DSPEC\_LP64





# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Dec-2021

**Hardware Availability:** Nov-2021

**Software Availability:** Dec-2020

## Base Optimization Flags

C benchmarks:

```
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-mbranches-within-32B-boundaries
```

Fortran benchmarks:

```
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
-mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib  
-ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

icc

644.nab\_s: icx

Fortran benchmarks:

ifort

Benchmarks using both Fortran and C:

ifort icc

Benchmarks using Fortran, C, and C++:

icpc icc ifort



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

SPECspeed®2017\_fp\_base = 173

SPECspeed®2017\_fp\_peak = 174

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Dec-2021

**Hardware Availability:** Nov-2021

**Software Availability:** Dec-2020

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

619.lbm\_s: basepeak = yes

638.imagick\_s: basepeak = yes

644.nab\_s: -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math  
-flto -mfpmath=sse -funroll-loops -fiopenmp  
-DSPEC\_OPENMP -qopt-mem-layout-trans=4  
-fimf-accuracy-bits=14:sqrt  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves\_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)  
-DSPEC\_SUPPRESS\_OPENMP -DSPEC\_OPENMP -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d\_s: Same as 603.bwaves\_s

654.roms\_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf\_s: basepeak = yes

627.cam4\_s: basepeak = yes

628.pop2\_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN\_s: basepeak = yes



# SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Hewlett Packard Enterprise**

(Test Sponsor: HPE)

**Synergy 480 Gen10 Plus**

(3.00 GHz, Intel Xeon Gold 6354)

**SPECspeed®2017\_fp\_base = 173**

**SPECspeed®2017\_fp\_peak = 174**

**CPU2017 License:** 3

**Test Sponsor:** HPE

**Tested by:** HPE

**Test Date:** Dec-2021

**Hardware Availability:** Nov-2021

**Software Availability:** Dec-2020

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revG.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-21 00:03:53-0500.

Report generated on 2022-01-18 18:57:59 by CPU2017 PDF formatter v6442.

Originally published on 2022-01-18.