



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

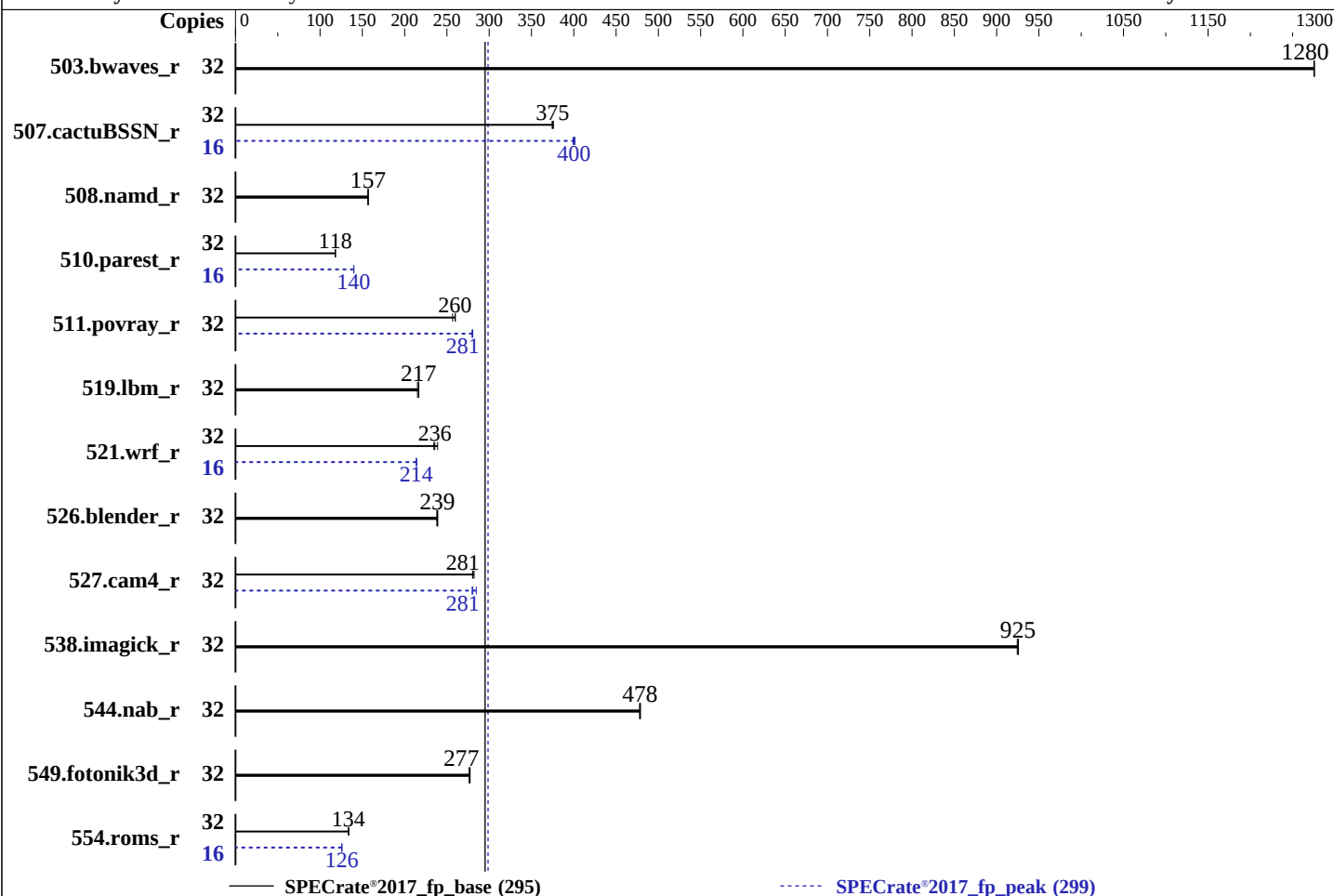
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024



Hardware

CPU Name: Intel Xeon 6714P
Max MHz: 4300
Nominal: 4000
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1,2 chips
Cache L1: 64 KB I + 48 KB D on chip per core
L2: 2 MB I+D on chip per core
L3: 48 MB I+D on chip per chip
Other: None
Memory: 1 TB (16 x 64 GB 2Rx4 PC5-6400B-R)
Storage: 1 x 445 GB SATA SSD
Other: CPU Cooling: Air

Software

OS: SUSE Linux Enterprise Server 15 SP6 6.4.0-150600.21-default
Compiler: C/C++: Version 2024.1 of Intel oneAPI DPC++/C++ Compiler for Linux;
Fortran: Version 2024.1 of Intel Fortran Compiler for Linux;
Parallel: No
Firmware: Version 4.3.6a released Mar-2025
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	32	<u>252</u>	<u>1280</u>	252	1280	252	1280	32	<u>252</u>	<u>1280</u>	252	1280	252	1280
507.cactuBSSN_r	32	<u>108</u>	<u>375</u>	108	374	108	376	16	<u>50.6</u>	<u>400</u>	50.7	399	50.5	401
508.namd_r	32	<u>194</u>	<u>157</u>	194	157	194	157	32	<u>194</u>	<u>157</u>	194	157	194	157
510.parest_r	32	<u>709</u>	<u>118</u>	709	118	709	118	16	<u>299</u>	<u>140</u>	299	140	299	140
511.povray_r	32	291	257	<u>288</u>	<u>260</u>	287	260	32	267	280	<u>266</u>	<u>281</u>	266	281
519.lbm_r	32	156	217	<u>156</u>	<u>217</u>	157	215	32	156	217	<u>156</u>	<u>217</u>	157	215
521.wrf_r	32	306	235	<u>304</u>	<u>236</u>	300	239	16	168	214	<u>168</u>	<u>214</u>	167	214
526.blender_r	32	205	238	<u>204</u>	<u>239</u>	204	239	32	205	238	<u>204</u>	<u>239</u>	204	239
527.cam4_r	32	<u>199</u>	<u>281</u>	200	280	198	282	32	200	280	197	285	<u>199</u>	<u>281</u>
538.imagick_r	32	<u>86.0</u>	<u>925</u>	86.1	924	86.0	926	32	<u>86.0</u>	<u>925</u>	86.1	924	86.0	926
544.nab_r	32	<u>113</u>	<u>478</u>	113	478	112	479	32	<u>113</u>	<u>478</u>	113	478	112	479
549.fotonik3d_r	32	451	276	449	277	<u>451</u>	<u>277</u>	32	451	276	449	277	<u>451</u>	<u>277</u>
554.roms_r	32	<u>380</u>	<u>134</u>	380	134	381	134	16	<u>202</u>	<u>126</u>	202	126	202	126

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

General Notes (Continued)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)

is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS settings:

Hardware prefetcher set to Enabled

Adjacent cache line prefetcher set to Disabled

Patrol scrub set to Disabled

LLC prefetch set to Enabled

XPT prefetch set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197

running on c240m8-spec1 Tue Jun 17 05:13:55 2025

SUT (System Under Test) info as seen by some common utilities.

Table of contents

-
1. uname -a
 2. w
 3. Username
 4. ulimit -a
 5. sysinfo process ancestry
 6. /proc/cpuinfo
 7. lscpu
 8. numactl --hardware
 9. /proc/meminfo
 10. who -r
 11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)
 12. Services, from systemctl list-unit-files
 13. Linux kernel boot-time arguments, from /proc/cmdline
 14. cpupower frequency-info
 15. tuned-adm active
 16. sysctl
 17. /sys/kernel/mm/transparent_hugepage
 18. /sys/kernel/mm/transparent_hugepage/khugepaged
 19. OS release
 20. Disk information
 21. /sys/devices/virtual/dmi/id
 22. dmidecode
 23. BIOS
-
1. uname -a
Linux c240m8-spec1 6.4.0-150600.21-default #1 SMP PREEMPT_DYNAMIC Thu May 16 11:09:22 UTC 2024 (36c1e09)
x86_64 x86_64 x86_64 GNU/Linux
-

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

2. w

```
05:13:55 up 2:48, 2 users, load average: 0.02, 0.02, 3.07
USER      TTY      FROM          LOGIN@      IDLE        JCPU        PCPU        WHAT
root      tty1      -             02:27       2.00s       0.81s       0.01s      -bash
```

3. Username

From environment variable \$USER: root

4. ulimit -a

```
core file size          (blocks, -c) unlimited
data seg size           (kbytes, -d) unlimited
scheduling priority     (-e) 0
file size                (blocks, -f) unlimited
pending signals         (-i) 4125149
max locked memory       (kbytes, -l) 8192
max memory size         (kbytes, -m) unlimited
open files              (-n) 1024
pipe size               (512 bytes, -p) 8
POSIX message queues    (bytes, -q) 819200
real-time priority      (-r) 0
stack size              (kbytes, -s) unlimited
cpu time                (seconds, -t) unlimited
max user processes      (-u) 4125149
virtual memory          (kbytes, -v) unlimited
file locks              (-x) unlimited
```

5. sysinfo process ancestry

```
/usr/lib/systemd/systemd --switched-root --system --deserialize=42
login -- root
-bash
-bash
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=32 -c
ic2024.1-lin-sapphirerapids-rate-20240308.cfg --define smt-on --define cores=16 --define physicalfirst
--define invoke_with_interleave --define drop_caches --tune base,peak -n 3 -o all fprate
runcpu --nobuild --action validate --define default-platform-flags --define numcopies=32 --configfile
ic2024.1-lin-sapphirerapids-rate-20240308.cfg --define smt-on --define cores=16 --define physicalfirst
--define invoke_with_interleave --define drop_caches --tune base,peak --iterations 3 --output_format all
--nopower --runmode rate --tune base:peak --size refrate fprate --nopreenv --note-preenv --logfile
$SPEC/tmp/CPU2017.393/temlogs/preenv.fprate.393.0.log --lognum 393.0 --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017
```

6. /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) 6714P
vendor_id      : GenuineIntel
cpu family     : 6
model          : 173
stepping       : 1
microcode      : 0x1000380
bugs           : spectre_v1 spectre_v2 spec_store_bypass swapgs bhi
cpu cores      : 8
siblings       : 16
2 physical ids (chips)
32 processors (hardware threads)
physical id 0: core ids 0-7
physical id 1: core ids 0-7
```

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

physical id 0: apicids 0-15

physical id 1: apicids 128-143

Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for virtualized systems. Use the above data carefully.

7. lscpu

From lscpu from util-linux 2.39.3:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Address sizes:         46 bits physical, 57 bits virtual
Byte Order:            Little Endian
CPU(s):                32
On-line CPU(s) list:   0-31
Vendor ID:             GenuineIntel
BIOS Vendor ID:        Intel(R) Corporation
Model name:            Intel(R) Xeon(R) 6714P
BIOS Model name:       Intel(R) Xeon(R) 6714P  CPU @ 4.0GHz
BIOS CPU family:       179
CPU family:            6
Model:                 173
Thread(s) per core:    2
Core(s) per socket:    8
Socket(s):              2
Stepping:              1
CPU(s) scaling MHz:    42%
CPU max MHz:           4300.0000
CPU min MHz:           800.0000
BogoMIPS:              8000.00
Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat
                        pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
                        pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good
                        nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni
                        pclmulqdq dtes64 monitor ds_cpl smx est tm2 ssse3 sdbg fma cx16 xtpr
                        pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer
                        aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb
                        cat_l3 cat_l2 cdp_l3 intel_ppin cdp_l2 ssbd mba ibrs ibpb stibp
                        ibrs_enhanced fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
                        invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma
                        clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt
                        xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
                        cqm_mbm_local split_lock_detect user_shstk avx_vnni avx512_bf16
                        wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
                        hwp_pkg_req avx512vbmi umip pku ospke waitpkg avx512_vbmi2 gfni vaes
                        vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid
                        bus_lock_detect cldemote movdiri movdir64b enqcmd fsrm md_clear
                        serialize tsxldtrk pconfig arch_lbr ibt amx_bf16 avx512_fp16 amx_tile
                        amx_int8 flush_l1d arch_capabilities
L1d cache:             768 KiB (16 instances)
L1i cache:             1 MiB (16 instances)
L2 cache:              32 MiB (16 instances)
L3 cache:              96 MiB (2 instances)
NUMA node(s):          2
NUMA node0 CPU(s):     0-7,16-23
NUMA node1 CPU(s):     8-15,24-31
Vulnerability Gather data sampling: Not affected
Vulnerability Itlb multihit:      Not affected
Vulnerability L1tf:             Not affected
Vulnerability Mds:             Not affected
```

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

Vulnerability Meltdown: Not affected
Vulnerability Mmio stale data: Not affected
Vulnerability Reg file data sampling: Not affected
Vulnerability Retbleed: Not affected
Vulnerability Spec rstack overflow: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced / Automatic IBRS; IBPB conditional; RSB filling; PBRSE-eIBRS Not affected; BHI BHI_DIS_S
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	768K	12	Data	1	64	1	64
L1i	64K	1M	16	Instruction	1	64	1	64
L2	2M	32M	16	Unified	2	2048	1	64
L3	48M	96M	16	Unified	3	49152	1	64

8. numactl --hardware

NOTE: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0-7,16-23
node 0 size: 515234 MB
node 0 free: 513817 MB
node 1 cpus: 8-15,24-31
node 1 size: 516079 MB
node 1 free: 514711 MB
node distances:
node 0 1
0: 10 21
1: 21 10

9. /proc/meminfo

MemTotal: 1056065376 kB

10. who -r

run-level 3 Jun 17 02:25

11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)

Default Target Status
multi-user running

12. Services, from systemctl list-unit-files

STATE	UNIT FILES
enabled	YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron display-manager getty@ irqbalance issue-generator kbdsettings klog lvm2-monitor nsd postfix purge-kernels rollback rsyslog sep5 smartd sshd systemd-pstore wicked wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime	systemd-remount-fs
disabled	autofs autostart-initscripts blk-availability boot-sysctl ca-certificates chrony-wait chronyd console-getty cups cups-browsed debug-shell ebttables exchange-bmc-os-info firewallld fsidd gpm grub2-once haveged ipmi ipmievd issue-add-ssh-keys kexec-load lunmask man-db-create multipathd nfs nfs-blkmap rpcbind rpmconfigcheck rsyncd serial-getty@ smartd_generate_opts snmpd snmptrapd systemd-boot-check-no-failures systemd-confext

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

indirect systemd-network-generator systemd-sysext systemd-time-wait-sync systemd-timesyncd tuned
udisks2 vncserver@
systemd-userdbd wickedd

13. Linux kernel boot-time arguments, from /proc/cmdline

BOOT_IMAGE=/boot/vmlinuz-6.4.0-150600.21-default
root=UUID=52f44b73-418f-485e-abb1-6b40f358d6a0
splash=silent
mitigations=auto
quiet
security=apparmor

14. cpupower frequency-info

analyzing CPU 1:
current policy: frequency should be within 800 MHz and 4.30 GHz.
The governor "performance" may decide which speed to use within this range.
boost state support:
Supported: yes
Active: yes

15. tuned-adm active

Current active profile: latency-performance

16. sysctl

kernel.numa_balancing	1
kernel.randomize_va_space	2
vm.compaction_proactiveness	20
vm.dirty_background_bytes	0
vm.dirty_background_ratio	3
vm.dirty_bytes	0
vm.dirty_expire_centisecs	3000
vm.dirty_ratio	20
vm.dirty_writeback_centisecs	500
vm.dirtytime_expire_seconds	43200
vm.extfrag_threshold	500
vm.min_unmapped_ratio	1
vm.nr_hugepages	0
vm.nr_hugepages_mempolicy	0
vm.nr_overcommit_hugepages	0
vm.swappiness	10
vm.watermark_boost_factor	15000
vm.watermark_scale_factor	10
vm.zone_reclaim_mode	0

17. /sys/kernel/mm/transparent_hugepage

defrag	always defer defer+madvise [madvise] never
enabled	[always] madvise never
hpage_pmd_size	2097152
shmem_enabled	always within_size advise [never] deny force

18. /sys/kernel/mm/transparent_hugepage/khugepaged

alloc_sleep_millisecs	60000
defrag	1

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Platform Notes (Continued)

max_ptes_none 511
max_ptes_shared 256
max_ptes_swap 64
pages_to_scan 4096
scan_sleep_millisecs 10000

19. OS release

From /etc/*-release /etc/*-version
os-release SUSE Linux Enterprise Server 15 SP6

20. Disk information

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 445G 57G 389G 13% /

21. /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc
Product: UCSC-C240-M8SX
Serial: WZP28449MSW

22. dmidecode

Additional information from dmidecode 3.4 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
16x 0xCE00 M321R8GA0PB2-CCPEC 64 GB 2 rank 6400

23. BIOS

(This section combines info from /sys/devices and dmidecode.)

BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M8.4.3.6a.0.0319250402
BIOS Date: 03/19/2025
BIOS Revision: 5.35

Compiler Version Notes

C | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

C++, C | 511.povray_r(base, peak) 526.blender_r(base, peak)

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

=====

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.
Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

=====

Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

=====

Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Benchmarks using both Fortran and C:

ifx icx

Benchmarks using both C and C++:

icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifx



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:

-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:

-w -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:

-w -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:

-w -std=c++14 -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):

-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:

-w -m64 -std=c++14 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Benchmarks using both Fortran and C:

ifx icx

Benchmarks using both C and C++:

icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifx

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Peak Optimization Flags (Continued)

538.imagick_r: basepeak = yes

544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids
-Ofast -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mprefer-vector-width=512
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:

503.bwaves_r: basepeak = yes

549.fotonik3d_r: basepeak = yes

554.roms_r: -w -m64 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:

-w -m64 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-Wno-implicit-int -mprefer-vector-width=512 -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:

511.povray_r: -w -std=c++14 -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast -xCORE-AVX512 -ffast-math -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -Wno-implicit-int
-mprefer-vector-width=512 -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

-w -m64 -std=c++14 -std=c11 -Wl,-z,muldefs -xsapphirerapids -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops

(Continued on next page)



SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2025 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M8 (Intel Xeon 6714P 4.0 GHz processor)

SPECrate®2017_fp_base = 295

SPECrate®2017_fp_peak = 299

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jun-2025

Hardware Availability: Feb-2025

Software Availability: Jun-2024

Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):

```
-qopt-mem-layout-trans=4 -Wno-implicit-int -mprefer-vector-width=512  
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc  
-L/usr/local/jemalloc64-5.0.1/lib
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-GNR-revE.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-GNR-revE.xml>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2025-06-17 08:13:54-0400.

Report generated on 2025-07-16 11:07:25 by CPU2017 PDF formatter v6716.

Originally published on 2025-07-15.