



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

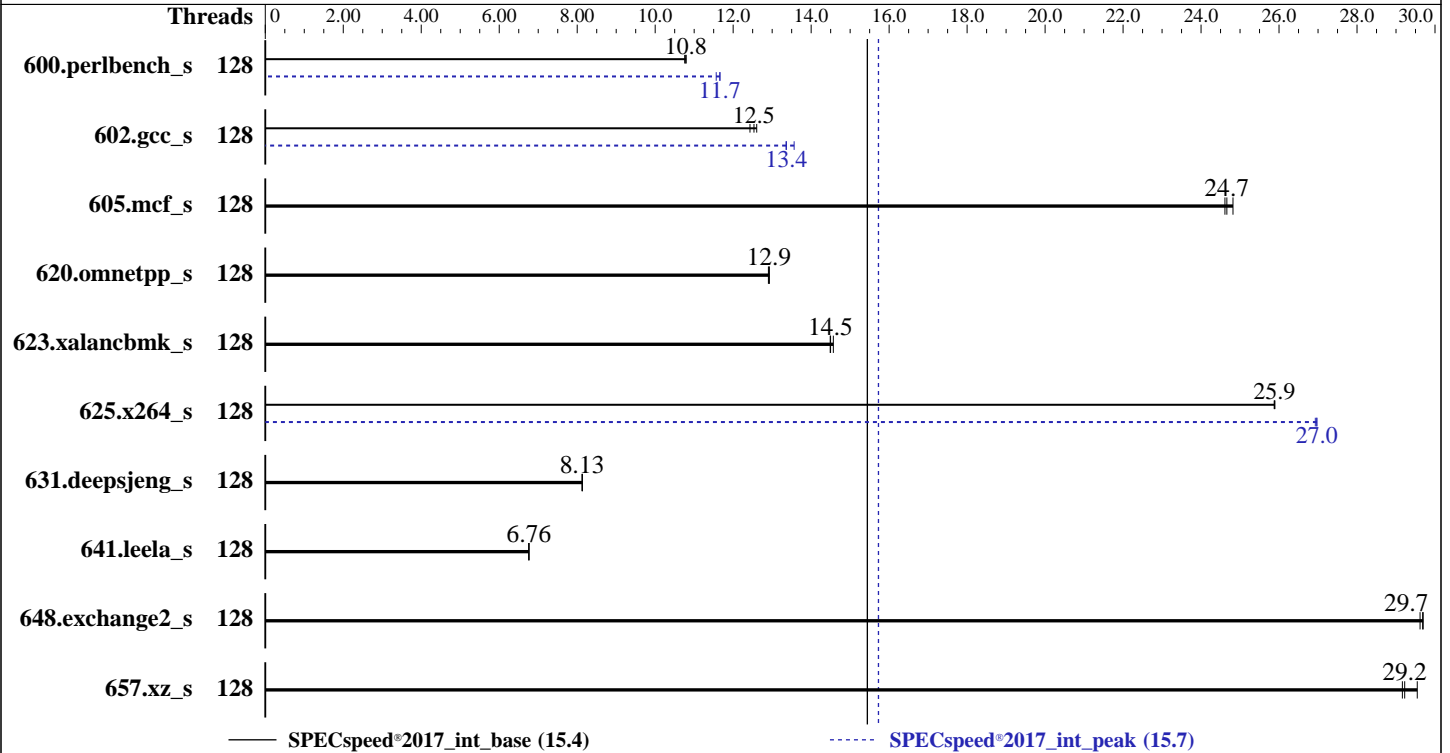
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025



Hardware

CPU Name: Intel Xeon 6724P
 Max MHz: 4300
 Nominal: 3600
 Enabled: 64 cores, 4 chips, 2 threads/core
 Orderable: 2,4 Chips
 Cache L1: 64 KB I + 48 KB D on chip per core
 L2: 2 MB I+D on chip per core
 L3: 72 MB I+D on chip per chip
 Other: None
 Memory: 2 TB (32 x 64 GB 2Rx4 PC5-6400B-R)
 Storage: 1 x 400 GB NVME SSD
 Other: CPU Cooling: Air

Software

OS: SUSE Linux Enterprise Server 15 SP6
 6.4.0-150600.21-default
 Compiler: C/C++: Version 2025.2 of Intel oneAPI DPC++/C++
 Compiler for Linux;
 Fortran: Version 2025.2 of Intel Fortran Compiler
 for Linux;
 Parallel: Yes
 Firmware: Version 6.0.2b released Jan-2026
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS and OS set to prefer performance
 at the cost of additional power usage



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2026
Hardware Availability: May-2025
Software Availability: Jun-2025

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	128	165	10.8	164	10.8	165	10.8	128	152	11.7	153	11.6	152	11.7
602.gcc_s	128	316	12.6	320	12.4	318	12.5	128	298	13.4	298	13.4	294	13.6
605.mcf_s	128	190	24.8	192	24.6	191	24.7	128	190	24.8	192	24.6	191	24.7
620.omnetpp_s	128	126	12.9	126	12.9	126	12.9	128	126	12.9	126	12.9	126	12.9
623.xalancbmk_s	128	97.7	14.5	97.3	14.6	97.8	14.5	128	97.7	14.5	97.3	14.6	97.8	14.5
625.x264_s	128	68.1	25.9	68.1	25.9	68.2	25.9	128	65.4	27.0	65.4	27.0	65.5	26.9
631.deepsjeng_s	128	176	8.13	176	8.13	176	8.13	128	176	8.13	176	8.13	176	8.13
641.leela_s	128	252	6.76	252	6.76	252	6.76	128	252	6.76	252	6.76	252	6.76
648.exchange2_s	128	99.3	29.6	99.0	29.7	99.0	29.7	128	99.3	29.6	99.0	29.7	99.0	29.7
657.xz_s	128	209	29.5	212	29.2	212	29.2	128	209	29.5	212	29.2	212	29.2

SPECspeed®2017_int_base = **15.4**

SPECspeed®2017_int_peak = **15.7**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM memory using Red Hat Enterprise Linux 8.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5 sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

Platform Notes

BIOS settings:

Hardware prefetcher set to Enabled
Adjacent cache line prefetcher set to Enabled
Patrol scrub set to Disabled
XPT prefetch set to Auto
LLC prefetch set to Enabled
Enhanced CPU performance set to Auto

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197
running on localhost Tue Apr 7 22:03:24 2026

SUT (System Under Test) info as seen by some common utilities.

Table of contents

1. uname -a
2. w
3. Username
4. ulimit -a
5. sysinfo process ancestry
6. /proc/cpuinfo
7. lscpu
8. numactl --hardware
9. /proc/meminfo
10. who -r
11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)
12. Failed units, from systemctl list-units --state=failed
13. Services, from systemctl list-unit-files
14. Linux kernel boot-time arguments, from /proc/cmdline
15. cpupower frequency-info
16. tuned-adm active
17. sysctl
18. /sys/kernel/mm/transparent_hugepage
19. /sys/kernel/mm/transparent_hugepage/khugepaged
20. OS release
21. Disk information
22. /sys/devices/virtual/dmi/id
23. dmidecode
24. BIOS

1. uname -a
Linux localhost 6.4.0-150600.21-default #1 SMP PREEMPT_DYNAMIC Thu May 16 11:09:22 UTC 2024 (36c1e09)
x86_64 x86_64 x86_64 GNU/Linux

2. w

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2026
Hardware Availability: May-2025
Software Availability: Jun-2025

Platform Notes (Continued)

```
22:03:24 up 20 min, 2 users, load average: 0.00, 0.00, 0.00
USER      TTY      FROM          LOGIN@      IDLE        JCPU        PCPU        WHAT
root      pts/0    10.29.148.201 22:02       4.00s      0.87s      0.00s      -bash
```

3. Username
From environment variable \$USER: root

4. ulimit -a

core file size	(blocks, -c)	unlimited
data seg size	(kbytes, -d)	unlimited
scheduling priority	(-e)	0
file size	(blocks, -f)	unlimited
pending signals	(-i)	8254279
max locked memory	(kbytes, -l)	8192
max memory size	(kbytes, -m)	unlimited
open files	(-n)	1024
pipe size	(512 bytes, -p)	8
POSIX message queues	(bytes, -q)	819200
real-time priority	(-r)	0
stack size	(kbytes, -s)	unlimited
cpu time	(seconds, -t)	unlimited
max user processes	(-u)	8254279
virtual memory	(kbytes, -v)	unlimited
file locks	(-x)	unlimited

5. sysinfo process ancestry

```
/usr/lib/systemd/systemd --switched-root --system --deserialize=42
sshd: /usr/sbin/sshd -D [listener] 0 of 10-100 startups
sshd: root [priv]
sshd: root@pts/0
-bash
-bash
runcpu --nobuild --action validate --define default-platform-flags -c
ic2025.2-lin-graniterapids-speed-20250605.cfg --define cores=64 --tune base,peak -o all --define
intspeedaffinity --define smt-on --define drop_caches intspeed
runcpu --nobuild --action validate --define default-platform-flags --configfile
ic2025.2-lin-graniterapids-speed-20250605.cfg --define cores=64 --tune base,peak --output_format all
--define intspeedaffinity --define smt-on --define drop_caches --nopower --runmode speed --tune base:peak
--size refspped intspeed --nopreenv --note-preenv --logfile
$SPEC/tmp/CPU2017.106/templogs/preenv.intspeed.106.0.log --lognum 106.0 --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017
```

6. /proc/cpuinfo

```
model name      : Intel(R) Xeon(R) 6724P
vendor_id       : GenuineIntel
cpu family      : 6
model           : 173
stepping        : 1
microcode       : 0x1000405
bugs            : spectre_v1 spectre_v2 spec_store_bypass swapgs bhi
cpu cores       : 16
siblings        : 32
4 physical ids (chips)
128 processors (hardware threads)
physical id 0: core ids 0-15
```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

Platform Notes (Continued)

```

physical id 1: core ids 0-15
physical id 2: core ids 0-15
physical id 3: core ids 0-15
physical id 0: apicids 0-31
physical id 1: apicids 128-159
physical id 2: apicids 256-287
physical id 3: apicids 384-415

```

Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for virtualized systems. Use the above data carefully.

7. lscpu

From lscpu from util-linux 2.39.3:

```

Architecture:                x86_64
CPU op-mode(s):              32-bit, 64-bit
Address sizes:                46 bits physical, 57 bits virtual
Byte Order:                   Little Endian
CPU(s):                       128
On-line CPU(s) list:         0-127
Vendor ID:                    GenuineIntel
BIOS Vendor ID:              Intel(R) Corporation
Model name:                   Intel(R) Xeon(R) 6724P
BIOS Model name:             Intel(R) Xeon(R) 6724P  CPU @ 3.6GHz
BIOS CPU family:             179
CPU family:                   6
Model:                        173
Thread(s) per core:          2
Core(s) per socket:          16
Socket(s):                    4
Stepping:                     1
CPU(s) scaling MHz:          24%
CPU max MHz:                  4300.0000
CPU min MHz:                  800.0000
BogoMIPS:                     7200.00
Flags:                         fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat
                                pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx
                                pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good
                                nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni
                                pclmulqdq dtes64 monitor ds_cpl smx est tm2 ssse3 sdbg fma cx16 xtpr
                                pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer
                                aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb
                                cat_l3 cat_l2 cdp_l3 intel_ppin cdp_l2 ssbd mba ibrs ibpb stibp
                                ibrs_enhanced fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
                                invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma
                                clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt
                                xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
                                cqm_mbm_local split_lock_detect user_shstk avx_vnni avx512_bf16
                                wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
                                hwp_pkg_req avx512vbmi umip pku ospke waitpkg avx512_vbmi2 gfni vaes
                                vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid
                                bus_lock_detect cldemote movdiri movdir64b enqcmd fsrm md_clear
                                serialize tsxldtrk pconfig arch_lbr ibt amx_bf16 avx512_fp16 amx_tile
                                amx_int8 flush_ldl arch_capabilities

L1d cache:                    3 MiB (64 instances)
L1i cache:                    4 MiB (64 instances)
L2 cache:                     128 MiB (64 instances)
L3 cache:                     288 MiB (4 instances)
NUMA node(s):                 4
NUMA node0 CPU(s):           0-15,64-79

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2026
Hardware Availability: May-2025
Software Availability: Jun-2025

Platform Notes (Continued)

```

NUMA node1 CPU(s):          16-31,80-95
NUMA node2 CPU(s):          32-47,96-111
NUMA node3 CPU(s):          48-63,112-127
Vulnerability Gather data sampling: Not affected
Vulnerability Itlb multihit:   Not affected
Vulnerability Lltf:           Not affected
Vulnerability Mds:            Not affected
Vulnerability Meltdown:       Not affected
Vulnerability Mmio stale data: Not affected
Vulnerability Reg file data sampling: Not affected
Vulnerability Retbleed:       Not affected
Vulnerability Spec rstack overflow: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl
Vulnerability Spectre v1:     Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2:     Mitigation; Enhanced / Automatic IBRS; IBPB conditional; RSB filling;
                                PBRSB-eIBRS Not affected; BHI BHI_DIS_S
Vulnerability Srbds:          Not affected
Vulnerability Tsx async abort: Not affected

```

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	3M	12	Data	1	64	1	64
L1i	64K	4M	16	Instruction	1	64	1	64
L2	2M	128M	16	Unified	2	2048	1	64
L3	72M	288M	16	Unified	3	73728	1	64

8. numactl --hardware

NOTE: a numactl 'node' might or might not correspond to a physical chip.

```

available: 4 nodes (0-3)
node 0 cpus: 0-15,64-79
node 0 size: 515418 MB
node 0 free: 514708 MB
node 1 cpus: 16-31,80-95
node 1 size: 516048 MB
node 1 free: 515517 MB
node 2 cpus: 32-47,96-111
node 2 size: 516087 MB
node 2 free: 515274 MB
node 3 cpus: 48-63,112-127
node 3 size: 516041 MB
node 3 free: 514978 MB
node distances:
node  0  1  2  3
 0:  10  21  21  21
 1:  21  10  21  21
 2:  21  21  10  21
 3:  21  21  21  10

```

9. /proc/meminfo

MemTotal: 2113122468 kB

10. who -r

run-level 3 Apr 7 21:43

11. Systemd service manager version: systemd 254 (254.10+suse.84.ge8d77af424)

Default Target Status

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2026
Hardware Availability: May-2025
Software Availability: Jun-2025

Platform Notes (Continued)

multi-user degraded

12. Failed units, from systemctl list-units --state=failed

```
UNIT          LOAD  ACTIVE SUB    DESCRIPTION
* sep5.service loaded failed failed systemd script to load sep5 driver at boot time
```

13. Services, from systemctl list-unit-files

```
STATE          UNIT FILES
enabled        YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron display-manager getty@ irqbalance
                issue-generator kbdsettings klog lvm2-monitor nscd nvme-fc-boot-connections
                nvme-autoconnect postfix purge-kernels rollback rsyslog sep5 smartd sshd systemd-pstore
                wickedd wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime systemd-remount-fs
disabled       autofs autyast-initscripts blk-availability boot-sysctl ca-certificates chrony-wait
                chronyd console-getty cups cups-browsed debug-shell ebttables exchange-bmc-os-info
                firewallld fsidd gpm grub2-once haveged ipmi ipmievd issue-add-ssh-keys kexec-load lunmask
                man-db-create multipathd nfs nfs-blkmap rpcbind rpmconfigcheck rsyncd serial-getty@
                smartd_generate_opts snmpd snmptrapd systemd-boot-check-no-failures systemd-confext
                systemd-network-generator systemd-sysexit systemd-time-wait-sync systemd-timesyncd tuned
                udisks2 vncserver@
indirect       systemd-userdbd wickedd
```

14. Linux kernel boot-time arguments, from /proc/cmdline

```
BOOT_IMAGE=/boot/vmlinuz-6.4.0-150600.21-default
root=UUID=c9a29bb1-f95d-4e5a-816b-db69c8356128
mitigations=auto
quiet
security=apparmor
```

15. cpupower frequency-info

```
analyzing CPU 48:
  current policy: frequency should be within 800 MHz and 4.30 GHz.
                  The governor "performance" may decide which speed to use
                  within this range.

  boost state support:
    Supported: yes
    Active: yes
```

16. tuned-adm active

```
It seems that tuned daemon is not running, preset profile is not activated.
Preset profile: latency-performance
```

17. sysctl

```
kernel.numa_balancing          1
kernel.randomize_va_space      2
vm.compaction_proactiveness     20
vm.dirty_background_bytes       0
vm.dirty_background_ratio      10
vm.dirty_bytes                  0
vm.dirty_expire_centisecs      3000
vm.dirty_ratio                  20
vm.dirty_writeback_centisecs    500
vm.dirtytime_expire_seconds     43200
vm.extfrag_threshold            500
```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2026
Hardware Availability: May-2025
Software Availability: Jun-2025

Platform Notes (Continued)

```

vm.min_unmapped_ratio      1
vm.nr_hugepages            0
vm.nr_hugepages_mempolicy  0
vm.nr_overcommit_hugepages 0
vm.swappiness              60
vm.watermark_boost_factor  15000
vm.watermark_scale_factor  10
vm.zone_reclaim_mode       0

```

```

-----
18. /sys/kernel/mm/transparent_hugepage
defrag      always defer defer+madvice [madvice] never
enabled     [always] madvice never
hpage_pmd_size 2097152
shmem_enabled always within_size advise [never] deny force

```

```

-----
19. /sys/kernel/mm/transparent_hugepage/khugepaged
alloc_sleep_millisecs 60000
defrag                 1
max_ptes_none         511
max_ptes_shared       256
max_ptes_swap         64
pages_to_scan         4096
scan_sleep_millisecs  10000

```

```

-----
20. OS release
From /etc/*-release /etc/*-version
os-release SUSE Linux Enterprise Server 15 SP6

```

```

-----
21. Disk information
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/nvme0n1p2 btrfs 371G 27G 341G 8% /home

```

```

-----
22. /sys/devices/virtual/dmi/id
Vendor:      Cisco Systems Inc
Product:     UCSX-410C-M8
Serial:      FVH2920P0DV

```

```

-----
23. dmidecode
Additional information from dmidecode 3.4 follows.  WARNING: Use caution when you interpret this section.
The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the
"DMTF SMBIOS" standard.
Memory:
1x 0xCE00 M321R8GA0PB2-CCPEC 64 GB 2 rank 6400
18x 0xCE00 M321R8GA0PB2-CCPKC 64 GB 2 rank 6400
13x 0xCE00 M321R8GA0PB2-CCPPC 64 GB 2 rank 6400

```

```

-----
24. BIOS
(This section combines info from /sys/devices and dmidecode.)
BIOS Vendor:      Cisco Systems, Inc.
BIOS Version:     X410M8.6.0.2b.0.0130261958

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

Platform Notes (Continued)

BIOS Date: 01/30/2026
BIOS Revision: 5.35

Compiler Version Notes

C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak)
657.xz_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2025.2.0 Build 20250605
Copyright (C) 1985-2025 Intel Corporation. All rights reserved.

C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak)
641.leela_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2025.2.0 Build 20250605
Copyright (C) 1985-2025 Intel Corporation. All rights reserved.

Fortran | 648.exchange2_s(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2025.2.0 Build 20250605
Copyright (C) 1985-2025 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

Base Portability Flags (Continued)

631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-w -std=c11 -m64 -Wl,-z,muldefs -xgraniterapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -fiopenmp
-DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:

-w -std=c++14 -m64 -Wl,-z,muldefs -xgraniterapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fdelayed-template-parsing -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

-w -m64 -Wl,-z,muldefs -xgraniterapids -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx

Peak Portability Flags

Same as Base Portability Flags



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -w -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fiopenmp -DSPEC_OPENMP -fno-strict-overflow
-fno-strict-aliasing -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc
```

```
602.gc_s: -w -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fiopenmp -DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc
```

605.mcf_s: basepeak = yes

```
625.x264_s: -w -std=c11 -m64 -Wl,-z,muldefs -xgraniterapids -O3
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-fno-alias -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic2025-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V2.0-GNR-revI.html>



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2026 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS X410 M8 (Intel Xeon 6724P 3.6 GHz processor)

SPECspeed®2017_int_base = 15.4

SPECspeed®2017_int_peak = 15.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Apr-2026

Hardware Availability: May-2025

Software Availability: Jun-2025

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic2025-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V2.0-GNR-revI.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2026-04-08 01:03:24-0400.

Report generated on 2026-05-06 09:58:27 by CPU2017 PDF formatter v6716.

Originally published on 2026-05-05.